

## MODULATORS

**R. W. Bradford, P. C. Edwards, C. W. Olson, Editor, R. M. Rowe,  
W. T. Tomlin, F. T. Veldhuizen, and A. L. Williams**

This chapter describes two pulse modulators developed for the SLAC accelerator. The first is the "main modulator," one of which is associated with each high-power klystron. The second is the "sub-booster modulator," one of which is located in each of the thirty sectors of the machine to pulse a sub-booster drive klystron.

### 13-1 Main modulator

#### *History (CWO)*

During the initial design phase, several different types of modulators were considered. The one selected and built for the accelerator was the line-type modulator.<sup>1</sup> This was chosen not only because of its high efficiency and relatively low cost but also because of the large reservoir of practical experience on the line-type modulator which had accumulated at Stanford during the development of klystrons and earlier accelerators.

The original concept was to use eight large power supplies, each of which would be rated at approximately 3 MW output at 23 kV and would furnish dc on a common buss to thirty modulators. Each modulator was to have a fuse and a switch to disconnect it from the line for maintenance purposes. In addition, each modulator was to have a vacuum relay to remove it rapidly from the common dc buss in the event of switch tube faults. A power scavenging de- $Q$ 'ing system was to be included for fast regulation of the pulse-forming network voltage. Induction voltage regulators were to be used to regulate output voltage by feedback to the ac input.

Because spark gaps were not very reliable at 360 pulses/sec and would,

consequently, require considerable maintenance, the switching device considered for use in the modulators was the multigrid, mercury pool ignitron. No large single hydrogen thyratron capable of handling the specified power levels (65-MW peak, 75-kW average output) existed at that time. Initially, the ignitron appeared to be a good solution, but experiments revealed serious disadvantages such as excessive fault rate, excessive anode time delay, low holdoff voltage, short life, and complicated triggering. During the period of experimental work with ignitrons, the state of the art for hydrogen thyratrons was advancing, and, by 1963, tubes which would satisfy our requirements became available.

That same year, the large megawatt power supply concept was re-evaluated with respect to high-voltage stability during switch tube faults. It was recognized that large switch tubes will occasionally fault. During such occurrence a short circuit would be placed on the 23-kV supply. Although a vacuum relay would be incorporated to clear such faults, the buss voltage supplying the remaining twenty-nine modulators would vary during the fault duration. This would, in turn, cause the output of the modulators to change and klystron phase shift and power decrease to occur. A direct consequence of this phase shift and decrease in RF power would be degradation of the beam energy spectrum. This problem and the inflexibility of adjusting the voltage of individual modulators to compensate for different klystron perveances resulted in changing the design concept from large dc power supplies feeding many modulators to small ones for each modulator.

In the adopted system, ac power at 12.47 kV is fed the length of the accelerator into induction voltage regulators which step this voltage down to a selected value between 258 and 595 V. Each induction voltage regulator supplies ac power to sixteen modulators. This system provides improved isolation from modulator to modulator, better fault clearing because ac faults are easier to clear than dc faults, and the capability of making minor voltage adjustments on each modulator by changing primary taps on the local rectifier transformer to compensate for different klystron perveances.

### *General description (CWO)*

The modulator built for the two-mile accelerator, shown in Figs. 13-1 and 13-2, was designed by SLAC personnel and fabricated and assembled from SLAC-supplied drawings and specifications.

The modulator and its associated pulse transformer was designed to meet or exceed the performance specifications given in Table 13-1.

The SLAC modulator is called a "line-type modulator." It is so named because it uses a capacitance-inductance network (pulse-forming network) constructed so as to simulate electrically a transmission line. A simplified diagram of the modulator is shown in Fig. 13-3. The main pulse and charging circuits have been drawn in schematic form to aid in the explanation of these circuits.

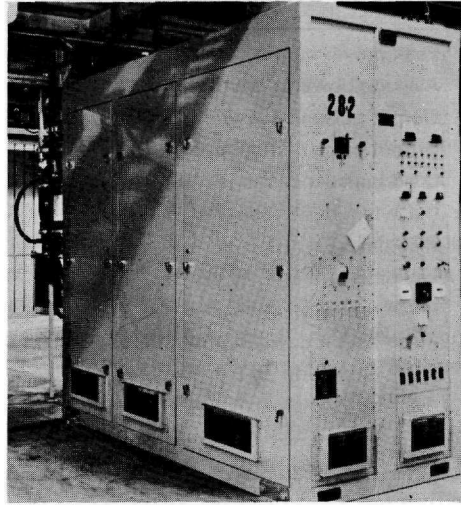
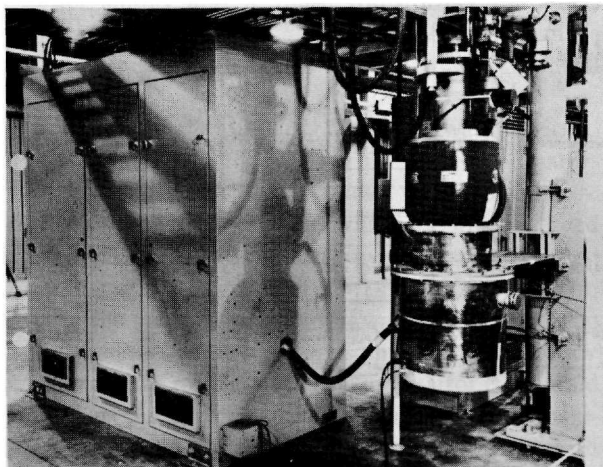


Figure 13-1 The SLAC modulator, view 1.

After each output pulse, the pulse-forming network (PFN) capacitors charge to approximately twice the dc power supply voltage because of the resonant charging characteristics of the charging transformer and the total PFN capacitance. The charging current flows from power supply ground, through the primary of the pulse transformer, the PFN inductors, the charging diodes, and the charging transformer to the positive side of the dc power supply. Because of the low values of inductances of the pulse

Figure 13-2 The SLAC modulator, view 2.

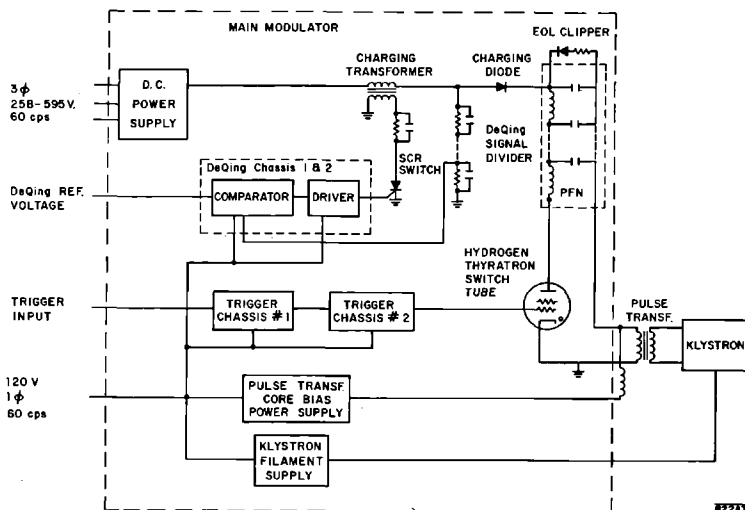


**Table 13-1 Overall specifications of modulator (including pulse transformer)**

Peak power output (max)	65 MW
Average power output (max)	75 kW
Output pulse voltage range	150–250 kV
Output pulse current range	110–262 A
Load impedance range	1365–955 ohms
Pulse length, flat top	2.5 $\mu$ sec
Rise time	0.7 $\mu$ sec
Fall time	1.2 $\mu$ sec
Pulse repetition rates	360, 180, 120, 60 pulses/sec
Pulse height deviation from flatness (max)	$\pm 0.5\%$
Pulse amplitude drift	
Long term	$\pm 1.5\%$ /hour
Short term	$\pm 0.25\%$ /5-min period
Time jitter	$\pm 10$ nsec

transformer primary and the PFN inductors, they have negligible effect on the charging cycle.

The PFN capacitor retains the voltage level of nearly twice the dc power supply voltage until the hydrogen switch tube is triggered. Once this occurs the PFN capacitors discharge through the primary of the pulse transformer, the switch tube, and PFN inductors. Since the reflected impedance of the klystron into the pulse transformer primary is approximately equal to the characteristic impedance of the PFN, half of the voltage on the PFN capacitors appears across the pulse transformer and half is dropped across the

**Figure 13-3 Block diagram of modulator.**

PFN. The time for complete discharge of the PFN is approximately  $3.5 \mu\text{sec}$ . Once the discharge is complete, the positive plate voltage on the hydrogen thyratron extinguishes and conduction ceases.

In addition to the main pulse and charging circuits described above there are additional supporting circuits as shown in Fig. 13-3. Trigger chassis Nos. 1 and 2 receive the input trigger pulse and shape and amplify it to the value required to trigger the hydrogen thyratron switch tube.

The de- $Q$ 'ing chassis in conjunction with the silicon controlled rectifier (SCR) switch and the charging transformer regulates the value of the charge placed on the PFN. If this charge were allowed to vary, the subsequent output pulse to the klystron would, in turn, be affected. Without some form of regulation any short-term ac line variations would show up as changes in the output of the dc supply which would cause the network charge and output voltage to vary accordingly.

The de- $Q$ 'ing circuitry regulates as follows. The PFN voltage is sampled by means of a voltage divider. This PFN voltage analog is fed to the comparator together with a dc reference voltage. The dc reference voltage is also fed to the variable voltage substitution (VVS), where it sets the level of the ac voltage fed to the modulators. When the sampled PFN voltage exceeds the dc reference voltage, the comparator generates an output pulse which is shaped by the driver chassis to trigger the SCR. The energy left in the charging transformer at the time the SCR conducts is dissipated in the secondary load resistor. The reverse blocking action of the charging diode causes the PFN voltage to be maintained at the value it had when the de- $Q$ 'ing circuit fired.

The de- $Q$ 'ing circuit is normally adjusted to dissipate a few percent of the charge in each cycle. It can, on a pulse-to-pulse and long-term basis, regulate the PFN voltage to 0.1% for line voltage changes of 3% or less, and for any repetition rate from 60 to 360 pulses/sec. Also, since the ac voltage from the VVS tracks the de- $Q$ 'ing reference voltage, the de- $Q$ 'ing system stays within range for all modulator output voltages.

A klystron filament power supply and a pulse transformer core bias supply are also included within the modulator. The output of both can be adjusted by controls and monitored by meters at the modulator's control panel.

The design, with the exception of the de- $Q$ 'ing circuitry, was patterned after conventional line-type modulators. Ideas from previous modulators procured from industry and from previous Stanford units were utilized.

The choice of the main high-voltage level in the modulator was governed by several factors. The major one was the ratings of the available switch tubes, which at the time the modulator was being designed, was 50 kV. In order to get the required rise time out of the pulse transformer, it was necessary to keep the turns ratio as low as possible. The klystron requires a maximum of 250 kV on its cathode. Therefore, using a turns ratio of 1:12, the modulator is required to produce a pulse of 21 kV. This pulse voltage demands about 40 kV maximum on the pulse-forming network which gives a comfortable margin with

50-kV thyratrons. Since the  $Q$  of the charging system is high, there is approximately 2:1 step-up in voltage from power supply to pulse-forming network. The power supply voltage required is, therefore, 20 kV plus about 3% for de- $Q$ 'ing. Approximately 5% "positive" mismatch is used at full voltage, i.e., the load impedance is about 5% higher than the PFN impedance.

The cabinet which measures 4 ft wide  $\times$  8 ft deep  $\times$  8 ft high is built of heavy gauge sheet steel. Three doors are provided on each long side to provide easy access to all components inside. Cooling for the components inside the cabinet is provided by three 1500-ft<sup>3</sup>/min fans mounted just below exhaust ports in the roof of the modulator.

Radio frequency interference (RFI) was recognized as a problem because of the high pulse voltages involved. Precautions are taken to minimize RFI originating from high-energy pulse radiation. The cabinet is divided into two parts, the high and the low noise regions, with a steel bulkhead separating the two. As much of the low level circuitry as possible is placed in the low noise part so as to minimize RFI pickup on its wiring. The doors are equipped with RFI metal gasketing so as to form good conductive seals around the door edges. In addition, latches are provided around the edges of the doors to force them against the gasketing thus providing better conduction between mating parts. The air intakes and exhaust ports are covered with RFI filters of the honeycomb type to prevent radiation through these openings. All wires, ac and control leads, passing through the top of the cabinet are filtered with RFI filters to reduce conducted noise.

The control panel contains all the necessary controls, meters, and interlock lights to operate the modulator. The main circuit breaker on the left control panel is used for fault protection as well as for connecting and disconnecting the modulator from the main feeder buss which feeds fifteen additional modulators. The modulator is sufficiently stable to make run-up from low voltage unnecessary. It may be placed on the line at any VVS voltage setting within the operating range. For maintenance purposes, an auxiliary power input socket on the left control panel, just above the air intake, is used to supply power to the modulator from a portable power source. Access to this socket is made by unlatching its protective cover with the same key that, upon removal, locks out the main circuit breaker. This provides personnel protection and, in addition, prevents simultaneous excitation from two power sources.

The lethal voltages present within the modulator when the unit is operating made it mandatory to incorporate a number of personnel safety features. The modulator has a total of six lock-equipped doors. The key for five of these doors is located inside the modulator on the support post adjacent to the left rear door. The key for the latter door is attached by welded ring to another key normally inserted into a key interlock mounted on the front control panel. In order to remove the two keys it is necessary to rotate the key interlock to the "off" position. This electrically opens the interlock and prevents excitation of the high voltage. When the left rear door is opened, a spring-loaded two sectional high-voltage shorting switch closes and places a short across the

filter and PFN capacitors. In addition, a door microswitch in series with the five remaining door interlocks releases and electrically opens the interlock chain. Grounding hooks are also provided inside each door with an attached cable that drapes across the door opening to remind the individual gaining access to use the hook to ground out any potentially hazardous circuits.

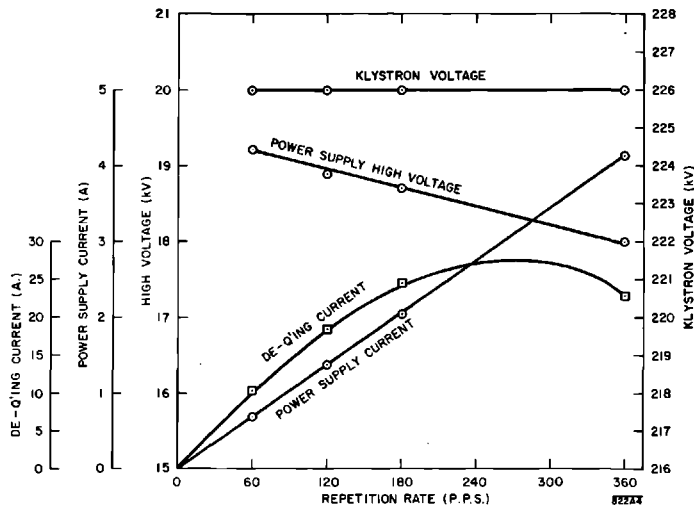
It was recognized early in the design phase that each modulator-klystron station would be subject to various faults during operation, such as klystron arcs, vacuum system gas bursts, thyratron faults, high-voltage power supply overloads, and end-of-line clipper overcurrents. A circuit was incorporated in the modulator interlock chain which works in conjunction with an external klystron protection chassis. It recycles the modulator up to a predetermined number of faults (from 1 to 15 as set by a rotary switch on the control panel) in 55 min. If the actual faults exceed the predetermined number in the 55-min period, the modulator is shut down automatically and must be reset manually. Faults external to the modulator merely interrupt the trigger for approximately 1 sec or longer in case of continuous faults. Faults originating in the modulator interrupt the high voltage by opening a contractor in the primary of the main rectifier transformer. If the fault clears in 1.5 sec, the high voltage is turned on automatically and operation is resumed.

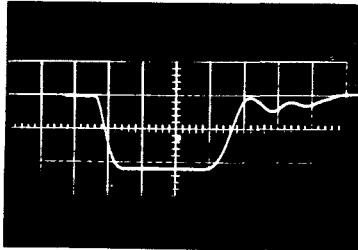
As can be seen in Fig. 13-2, the pulse transformer tank is external to the modulator cabinet and is an appendage hanging from the bottom of the klystron. A special triaxial cable feeds the pulse power from the modulator to the pulse transformer tank.

Figure 13-4 shows modulator-characteristic curves of the dc power supply output voltage and current, the de-Q'ing current, and the klystron beam voltage for various pulse repetition rates.

Figure 13-5 is an oscillogram of the klystron beam voltage pulse.

Figure 13-4 Modulator characteristics.





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1  $\mu$ s/div.  
122 kV/div.

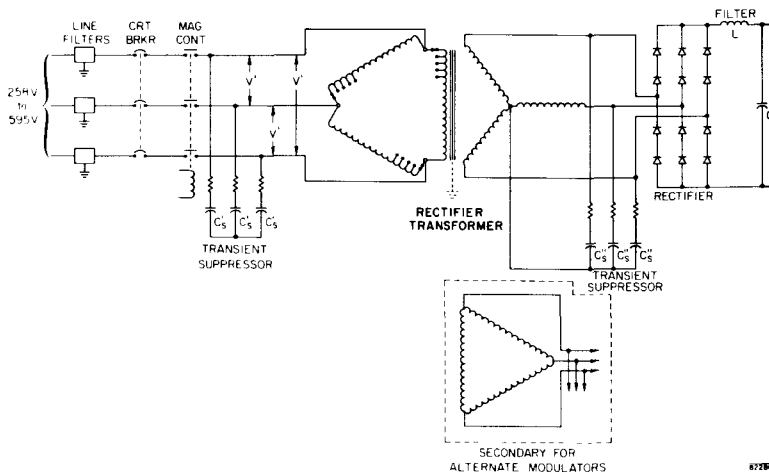
**Figure 13-5** Klystron beam voltage pulse.  
(Time scale: 1  $\mu$ sec/large division.)

*Modulator power supplies (PCE)*

The three-phase ac input to the modulator can be any level from 258 to 595 V, depending on the setting of the external induction voltage regulator. This regulator furnishes the ac power to a total of sixteen modulators. The input ac enters the modulator through three 125-A line filters which decouple high-frequency noise from the ac lines, thus preventing possible RFI.

The power supply used in the modulator is a conventional, three-phase, double-way, dc power supply. The three-phase variable voltage is delivered through a circuit breaker and contactor to a step-up rectifier transformer (see Fig. 13-6). The secondary of this transformer feeds power to a semiconductor rectifier assembly. The rectified output, proportional to the ac input, is delivered to the pulse-forming network via the inductance-capacitance (LC) rectifier filter and charging transformer.

**Figure 13-6** Schematic diagram of modulator power supply.



822B8



The rectifier transformer is an oil-filled, hermetically sealed, floor-mounted unit. It is rated to provide 3.8 A (rms) at 17.3 kV with 595 V in the primary. The primary has taps brought out to external terminals to allow reduction of dc output voltage in steps of 2.5, 5, 7.5, and 10%. The dc regulation is 8% (maximum) for a range from 5 to 100% full load. The reactance of the transformer was selected to be  $10 \pm 0.75\%$ . This fairly high leakage reactance was chosen to limit the load current during short circuit faults in order to protect rectifier units from damage. The transformer excitation does not exceed 5% at 595 V.

The secondary of the rectifier transformer is connected to a three-phase, double-way, semiconductor rectifier assembly. This assembly consists of six stacks of 100 silicon diodes, each capable of delivering 3 A average at 600 V. Each diode is paralleled with a resistance and a capacitor to equalize voltage distribution across the series string. The entire rectifier assembly is rated to deliver 23 kV at 4.5 A dc when the modulator is running at the maximum repetition rate of 360 pulses/sec.

The rectifier transformers for half of the 240 modulators are connected with a delta primary and a delta secondary while the remainder are connected delta-Y. The result is a phase shift in the harmonic currents of one group with respect to the other. The characteristic fifth and seventh harmonics of a six-phase rectifier effectively cancel one another.

Low-frequency transient suppressor networks are connected from line to line in the primary and secondary of the rectifier transformer. These suppressors not only reduce transients resulting from rectifier commutation action in the secondary but also prevent the occurrence of overvoltage caused by the interruption of exciting current in the primary.

If these transients are not suppressed, damage to the solid-state rectifier assembly can occur, and dielectric insulation failure can result from the repetition of transient overvoltages caused by the action of rectifier commutation. The capacitors in the primary suppressor are sized to maintain the transformer exciting current magnitude by resonating with the transformer's inductance at a frequency not greater than 60 cycles/sec for a short period after the primary voltage is disconnected from the transformer by opening the line circuit breaker. The transformer excitation and primary transient suppressor capacitor circuits are analyzed as follows:

1. The transformer excitation equivalent inductance for  $\Delta$  winding connection is calculated from

$$L_e = \sqrt{3} V' / 2\pi f I_e$$

where

$L_e$  = the equivalent inductance of the transformer excitation circuit in henrys

$I_e$  = the exciting current measured in the supply lines, rms amperes

$V'$  = the supply line to line voltage, rms volts

$f$  = the frequency (= 60 Hz)

2. The primary line to line suppressor capacitance,  $C'_s$ , is calculated from

$$C'_s = [(2\pi f)^2 L'_e]^{-1} \text{ farads}$$

The primary side suppressor circuit is connected in Y (with the neutral isolated). Therefore each capacitance has to be twice the value calculated from (2) above. The voltage rating of the capacitors is 660 V ac in order to provide sufficient safety factor. The transformer core loss serves as a damping feature for  $L'_e C$ , so that only a nominal value of resistance is needed in series with the suppressor capacitance to provide proper damping.

Transients due to rectifier commutation tend to cause ringing in the secondary circuit comprising the transformer winding leakage inductance and the coil inherent capacitance. The purpose of the secondary suppressors is not only to reduce this ringing frequency but also to damp the transient oscillation by the insertion of series resistance. Because resistance cannot be placed in a load current circuit, it is included in series with the capacitor. The secondary circuit is connected in Y with the neutral isolated. Thus, the suppressor is a series resistance-capacitance network shunted across the 17-kV lines. Analysis of the secondary circuit includes the following steps:

1. The capacitance  $C_2$ , reflected into the secondary from the suppressor capacitance  $C'_s$  in the primary, is given by

$$C_2 = \frac{2C'_s}{N^2}$$

where  $N$  = the secondary-to-primary turns ratio.

2. The secondary suppressor capacitance  $C''_s$  is calculated from

$$C'' = [(2\pi f_1)^2 L''_s]^{-1}$$

and

$$C_s = [(2\pi f_0)^2 L''_s]^{-1}$$

where

$C''$  = the total capacitance formed by  $C_2$  in series with the parallel combination of the suppressor capacitance  $C''_s$  and  $C_s$

$L''_s$  = the equivalent transformer leakage inductance in henrys

$C_s$  = the coil inherent equivalent capacitance in farads

$f_1$  = the desired ringing frequency in hertz

$f_0$  = the natural frequency of the coil in hertz

Note that the transformer inherent frequency is typically 10–50 kHz, and  $C''/C_s = (f_0/f_1)^2$ . In order to reduce  $f_1$  by one order of magnitude to avoid frequencies within the  $L''_s C_s$  frequency bandwidth, the ratio  $C''/C_s$  has to be 100:1. The value of the damping resistance is calculated using  $R_s = 2(L''_s/C'')^{1/2}$  ohms, where  $R_s$  is the series damping resistance including the transformer equivalent copper load loss resistance.

The LC filter in the dc circuit performs two functions. It attenuates the 360-Hz rectifier ripple to an acceptable value and reduces the ac power line

**Table 13-2 Alternating current power-line harmonic currents at master substation**

<i>Pulse repetition rate (pulses/sec)</i>	<i>For harmonic<sup>a</sup> frequency (Hz):</i>									
	120	180	240	300	420	660	780	1380	1500	<i>Total rms</i>
360	0.3	0.5	—	0.7	0.5	0.2	0.2	0.8	0.6	1.5
180	0.4	0.4	0.3	0.4	0.2	0.1	0.1	0.4	0.3	1.2
60	0.8	0.3	0.2	0.3	0.2	—	—	0.2	0.2	1.1

<sup>a</sup> Harmonic current expressed as percent of 60-Hz full load current at 360 pulses/sec.

harmonics, which result from resonant charging of the modulator PFN to less than 3% (total rms) of full modulator line current. The largest harmonic current occurs at 120 Hz when the modulator is operating at 60 pulses/sec.

The ac power line harmonic currents associated with operation of the accelerator are individually less than 1% of the fundamental (60-Hz) line current when the modulator is operating at full load. Table 13-2 lists the harmonics resulting from accelerator runs at 360, 180, and 60 pulses/sec. The maximum of all the harmonics is 1.5% rms and occurs at 360 pulses/sec. These harmonics flowing in the power system source impedance produce a 3% distortion of the line frequency sine wave. This amount of distortion is acceptable from the standpoint of interference with communications and control systems.

Typical harmonic current characteristics of an individual modulator are shown in Fig. 13-7. The result of using delta-delta and delta-Y transformer connections together with a phase-shifting transformer in the variable voltage substation is shown in Figs. 13-8 and 13-9. These circuit arrangements and the 12.47-kV cable itself attenuate the harmonic currents so that the master substation carries only a small fraction of the harmonics generated by the individual rectifiers in each modulator. This can be seen by comparing Table 13-2 with Fig. 13-7. Typical harmonic voltages in the 12.47-kV distribution system that result from operating the modulators at 360 pulses/sec are shown in Fig. 13-10.

The total power demand of the modulator system when operating at a level which produces 20-GeV beam energy at 360 pulses/sec is 20.4 MW as listed in Table 13-3. The wattless reactive component required to supply core excitation for the VVS induction voltage regulators as well as that resulting from the rectifier commutation phase angle lag is 10.4 MVAR. Table 13-3 lists the overall accelerator power loads typical for various repetition rates. The power demand load for klystron gallery conventional facilities and auxiliaries is less when the klystrons are operating at 360 pulses/sec than it is when they are being pulsed at 180 or 60 pulses/sec because the waveguide heaters shut off when the heating from RF system losses is sufficient to

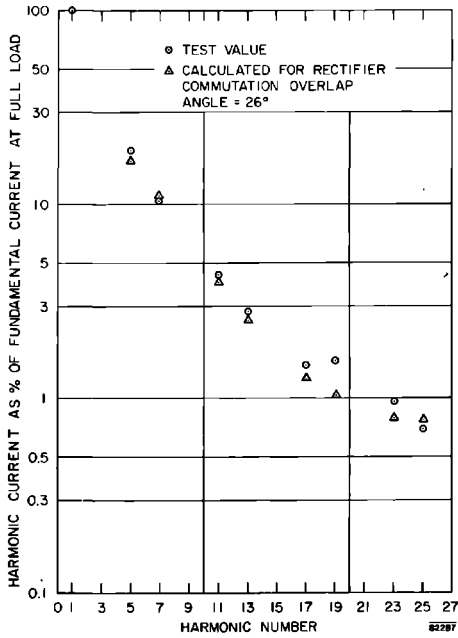


Figure 13-7 Individual modulator ac line-current harmonics.

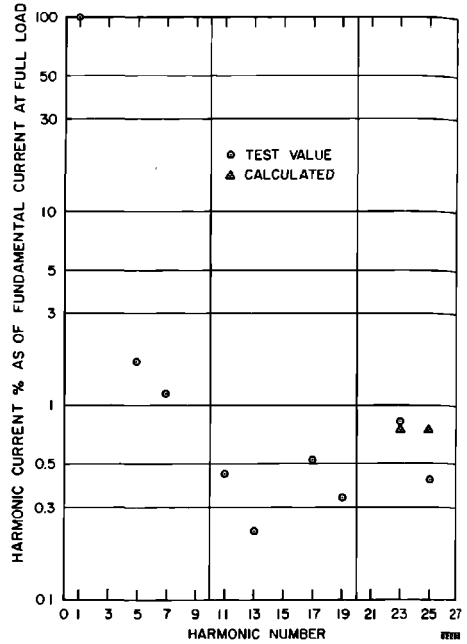


Figure 13-8 Plots of 12.47-kV line current harmonics at VVS input for 360 pulses/sec operation.

Figure 13-9 Plots of 12.47-kV line current harmonics at VVS input for 60 pulses/sec operation.

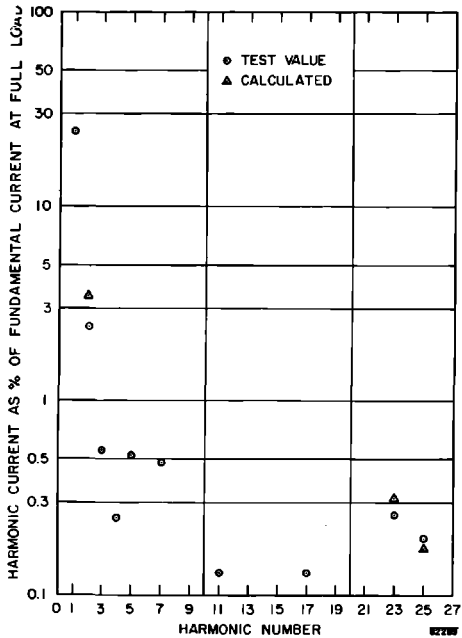
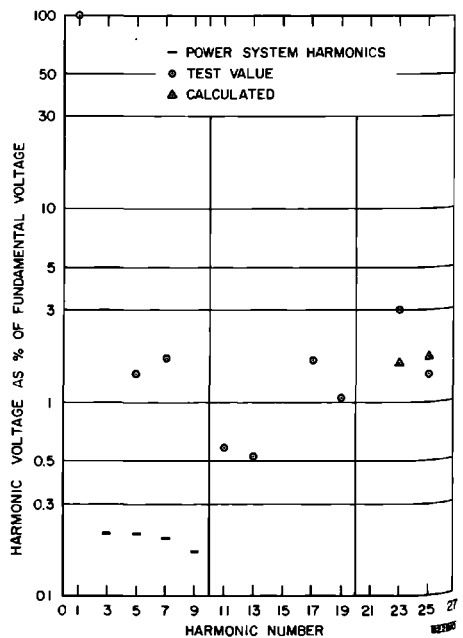


Figure 13-10 Plots of 12.47-kV line voltage harmonics at variable voltage substation input for 360 pps operation.



**Table 13-3 Alternating current power requirements<sup>a</sup> at master substation for 20 Gev**

<i>Pulse repetition rate (pulses/sec)</i>		<i>Power load (kW)</i>	<i>Reactive load (KVAR)</i>
360	Modulators (240) (ref. 105 V) plus injector	20,400	10,400
	Klystron gallery conventional facilities	4,141	1,900
	Total	24,541	12,300
180	Modulators (240) (ref. 105 V) plus injector	10,600	6,530
	Klystron gallery conventional facilities	5,128	1,870
	Total	15,728	8,400
60	Modulators (240) (ref. 105 V) plus injector	3,700	3,300
	Klystron gallery conventional facilities	5,128	1,870
	Total	8,828	5,170

<sup>a</sup> Not including cable or power factor correction capacitance.

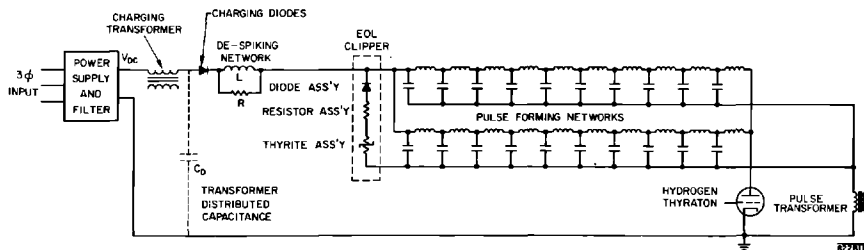
hold the temperature. At 360 pulses/sec and 105 V reference the VVS output voltage is 502 V, the current is 92 A, and the power demand is 75 kW per modulator.

#### *Pulse-forming network (ALW)*

The pulse applied to the high-power klystron is specified to be a maximum of 250 kV at 262 A, with a rise time of 0.7  $\mu$ sec, a fall time of 1.2  $\mu$ sec, and a duration of 2.5  $\mu$ sec, during which time the voltage is to be constant within  $\pm 0.5\%$ . The pulse is supplied by a pulse transformer, which is driven by the modulator.

To drive the primary of the pulse transformer, a two-terminal device, the PFN, is used. The PFN simulates the characteristics of a transmission line by the use of lumped capacitive and inductive elements. The PFN used in this modulator is a modified type-E circuit consisting of two parallel networks of ten fixed-value capacitors and ten essentially uncoupled slug-tuned inductors (see Fig. 13-11).

**Figure 13-11 Schematic diagram of simplified modulator.**



The PFN stores energy in the capacitors at a slow rate and discharges it rapidly in the form of a rectangular pulse of short duration when the hydrogen thyratron is triggered. The duration of the pulse and its approach to an ideal rectangular shape depends on the circuit constants of the PFN.

Although the circuit values of the individual  $LC$  sections for a particular pulse shape can be derived theoretically, it is much simpler to start off with the total value of capacitance and inductance required and experimentally derive the individual values. In a strictly theoretical approach, it is difficult to account for parameters such as stray capacitance and inductance that are always present in an actual circuit. In the PFN of this modulator, the total capacitance was derived from the energy equation below which states that the energy stored in the PFN before discharge must equal the energy supplied to the load, i.e.,

$$\frac{1}{2}CV_c^2 = \int_0^T V_p I_p dt$$

(13-1)

or

$$C = \frac{2V_p I_p T}{V_c^2}$$

where

$C$  = the total PFN capacitance

$V_c$  = the voltage across PFN capacitance (41.6 kV)

$V_p$  = the pulse transformer primary voltage (20.8 kV)

$I_p$  = the pulse transformer primary current (3000 A)

$T$  = the duration of pulse (3.35  $\mu$ sec, which includes the equivalent duration of rise and fall times).

The total inductance is found from the PFN characteristic impedance equation, viz.,

$$Z_0 = \left(\frac{L}{C}\right)^{1/2}$$

(13-2)

The choice of individual capacitance and inductance values and their number is influenced by previous knowledge of PFN characteristics. Pulse rise time is dependent on the number of  $LC$  sections. The greater the number, the faster the rise time. The way the leading edge turns into the flat top is mainly controlled by the value of the inductance nearest the switch tube. A comparatively large value for this coil rounds off the top of the leading edge. Small values give a sharp overshoot which trails off into the flat top. Flat-top irregularities are smoothed out by adjusting for symmetry between  $LC$  sections.

In this modulator it was determined that a dual ten-section PFN with fixed capacitors of approximately 0.014  $\mu$ F and tunable inductors of a

maximum inductance of  $4.5 \mu\text{H}$  would satisfy the pulse requirements. The dual section PFN was initially used in a split configuration, one section for each of two smaller switch tubes. When the large single switch tube became available, the two PFN's were paralleled. Had the single tube been available during the early design phase, a single ten-section PFN, with larger capacitors, would have been used. The use of tunable inductors allows adjustment over discrete portions of the output pulse. Pulse characteristics such as duration, rise time, droop, flat-top ripple, and fall time can be varied in a coarse manner by locating the interconnecting strap to the desired coil turn, and fine adjustments are made by varying the depth of insertion of a copper-tuning slug in the coil.

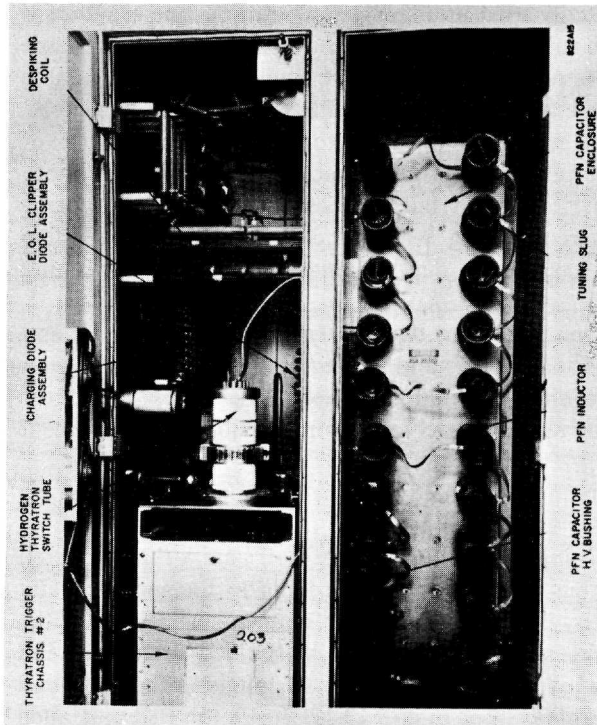
The fixed capacitors are specified to be between  $0.013$  and  $0.015 \mu\text{F}$  and  $50\text{-kV}$  operating voltage. The dielectric and impregnant used in these capacitors are polyethylene and silicone oil, respectively. The losses with these materials were found to be approximately one-third the losses in equivalent paper-oil capacitors.

The tunable inductors are mounted on the capacitor's high-voltage bushing stud. The inductor consists of ten turns of  $\frac{3}{8}$ -in. o.d. copper tubing with a center-to-center spacing of 4 in. and a length of 7 in. A three-fingered spacer of molded insulating material is mounted inside the inductor and supports a  $2\frac{1}{2}$ -in. diameter,  $5\frac{1}{8}$ -in. long, tubular copper slug. Each of the capacitor-inductor assemblies are interconnected by braided straps, one end of which is attached to the capacitor high-voltage bushing and the other end to the inductor using a cable clamp. Figure 13-12 shows the PFN installed in the modulator.

The PFN can be adjusted while the modulator is operating by installing in the modulator door opening a protective Lucite-wire screen. A Lucite tuning rod with a protective grounding ring midway along its length can be inserted through holes in this screen to adjust the copper tuning slugs.

#### *End-of-line clipper (ALW)*

The end-of-line clipper consists of a series combination of diodes, power resistors, and Thyrite resistors. (See Fig. 13-11.) The entire assembly is connected across the last (farthest removed from the switch tube) PFN capacitor. The function of the end-of-line clipper is to provide a low-impedance load for the collapsing field of the PFN inductors after a klystron fault. Without the end-of-line clipper, the excess energy on the PFN inductors would be transferred as an inverse charge to the PFN capacitors. Such a negative charge on the capacitors would have two adverse effects. The thyatron switch tube could be damaged by reverse arc-through and the PFN capacitors could be over voltaged (in the absence of de- $Q$ 'ing) during the next charging cycle. While accomplishing the objective of preventing a high inverse voltage being placed on the PFN capacitors after a load fault, the end-of-line clipper must present essentially an open circuit to the normal PFN positive charge and also



**Figure 13-12** Pulse-forming network, installed.

present a high impedance to the low inverse voltage required for thyatron deionization.

The diode section of the end-of-line clipper consists of a series string of one hundred and fifty resistance-capacitance ( $RC$ )-compensated, 600-V, 20-A silicon diodes. These diodes provide a low-impedance path for inverse voltages and essentially an open circuit to the normal PFN positive voltage.

The resistor assembly comprises four parallel legs of two 10-ohm, 200-W resistors in series to give an equivalent resistance of 5 ohms. These resistors along with the Thyrite assembly provide essentially a matched power dissipating load to the PFN for the high inverse charge.

The Thyrite assembly is made up of four parallel legs of six 6-in. diameter Thyrite disks in series. Thyrite is a nonlinear resistive material in which the resistance varies inversely as a power function of the voltage. With a negative deionization voltage of say, 3.6 kV the resistance of this Thyrite assembly is approximately 2 kohms. When the high negative fault voltage is impressed on the Thyrite assembly, the resistance drops to an extremely low value, and the



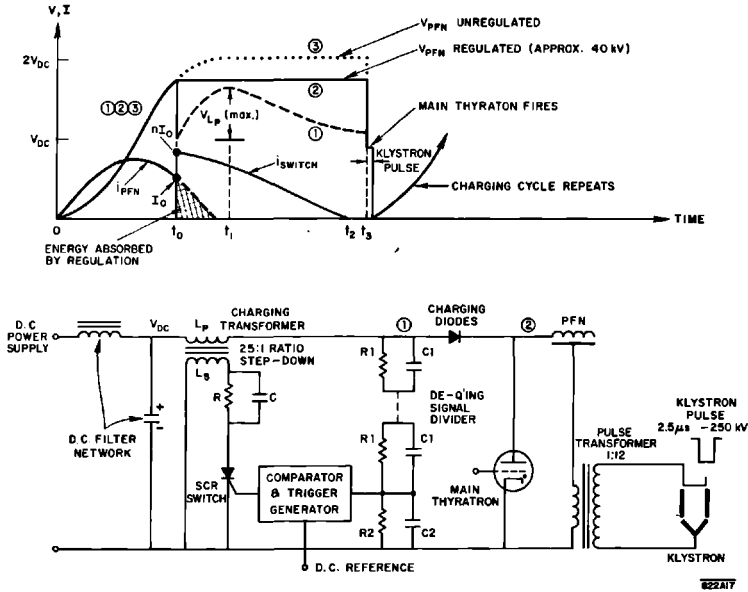
series combination of diodes, power resistors, and Thyrites provides a low impedance to dissipate the negative charge on the PFN. A monitoring device consisting of a current transformer-relay combination senses end-of-line clipper current each time a load fault occurs. In this event, the recycle circuit mentioned earlier in this chapter causes the modulator to be turned off for approximately 1.5 sec and then turned on again.

*Pulse-forming network voltage regulation (de-Q'ing) (WTT)*

Regulation of the klystron pulse voltage is accomplished by controlling the voltage to which the PFN is charged. This method, although somewhat indirect, is much simpler than working directly with the 250-kV klystron pulse. It has the disadvantage, however, that the actual regulation occurs sometime prior to pulsing the klystron, and leakage in the PFN capacitors or external leakage paths across the network will allow the PFN voltage to discharge slightly. In the SLAC modulators, operating from 60 to 360 pulses/sec, the time delay between regulation and pulsing varies from approximately 14.7 to 0.75 msec. As the discharge or leakage rate is constant, regulation is not affected at fixed repetition rates. The PFN voltage and, consequently, the klystron voltage will decrease slightly, however, when the repetition rate is changed from 360 to 60 pulses/sec.

Regulation against two causes of PFN voltage variation is necessary to insure klystron pulse stability. As the PFN voltage is a direct function of the dc power supply voltage (Eq. 13-5) and this, in turn, is proportional to the ac input voltage, any change in the input is reflected as a change in the PFN voltage. Although the modulators are fed in groups of sixteen by an induction voltage regulator, this unit has a minimum response time of several seconds and cannot regulate for pulse-to-pulse amplitude variations. The second need for regulation arises from either misfiring of the main thyatron during the charging cycle or arcing in the load during the output pulse. Either will result in an increase in PFN voltage for the succeeding charging cycle although the latter effect is greatly reduced by use of a negative discharge circuit (end-of-line clipper) for the PFN as discussed earlier.

A simplified diagram of the PFN charging and regulating circuits is shown in Fig. 13-13 along with the pertinent waveforms. In the conventional method of regulation or de-Q'ing, the charging transformer is a single-winding inductor shunted by a parallel RC network in series with a switch, usually a thyatron tube. Because the charging inductor voltage rises to approximately twice that of the dc power supply, the tube, its filament and reservoir transformers, and the RC network all rise to a very high voltage above ground, requiring large insulators and component separation. It is also necessary to insulate the tube from its trigger circuitry. Space was not available for insulating these components to 45 kV, so the step-down transformer circuit of Fig. 13-13 was developed. An additional advantage of the low-voltage regulating circuit was that a solid-state switch could be employed, offering longer life and more trouble-free operation.



**Figure 13-13 Pulse-forming network charging and regulating circuits with waveforms. Regulation occurs at  $t_0$ . Maximum silicon controlled rectifier switch current =  $nI_0$ , where  $n = 25$ .**

The operation of either circuit is basically the same, the major difference being the leakage inductance present in the charging transformer. For the lossless (infinite  $Q$ ) case, the charging current flowing into the PFN capacitors and the resultant voltages across the charging transformer primary and the PFN are given, respectively, by

$$i_{PFN} = \frac{V_{DC}}{\omega L_p} \sin \omega t \tag{13-3}$$

$$V_{L_p} = -L_p \frac{di_{PFN}}{dt} = -V_{DC} \cos \omega t \tag{13-4}$$

$$V_{PFN} = \frac{1}{C_{PFN}} \int_0^t i_{PFN} dt = V_{DC}(1 - \cos \omega t) \tag{13-5}$$

where  $\omega = (L_p C_{PFN})^{-1/2}$ , and  $L_p$  is the inductance of the charging transformer primary.

The charging current is restricted to a unidirectional flow by the presence of the charging diode and thus forms the basis for this method of regulation. If the current is forced to stop flowing into the PFN, then the voltage will remain at the level reached except for the small leakage present. This is accomplished by "loading" the charging transformer (or inductor) with a parallel resistor and capacitor. The voltage across the inductor then becomes a function primarily of its inductance, the magnitude of the current when the switch was

closed, and the added resistance and capacitance. Initially the uncharged capacitor in the secondary circuit appears as a short circuit and the voltage across the inductor drops to zero as shown in Fig. 13-13. It will then assume one of three possible forms, depending upon whether the  $R-L-C$  combination is overdamped, critically damped, or underdamped. Lowering the transformer primary voltage drop thus causes the anodes of the charging diodes to become negative with respect to their cathodes, and conduction ceases.

Considering the underdamped or damped oscillatory case with the resistance and capacitance reflected into the transformer primary, and assuming that current flow to the PFN is zero, the voltage across the inductance is given by

$$V_{L_p} = \frac{I_0}{\omega_0 C} \exp\left[-\frac{\omega_0(t-t_0)}{2\omega_0 RC}\right] \sin \omega_0(t-t_0) \quad (13-6)$$

where

$$\omega_0 = \left(\frac{1}{L_p C} - \frac{1}{4R^2 C^2}\right)^{1/2}$$

and

$$I_0 = \frac{V_{DC}}{\omega L_p} \sin \omega t_0$$

that is,  $I_0$  is the magnitude of the charging current  $i_{PFN}$  at the instant of regulation ( $t_0$  in Fig. 13-13). This analysis has neglected any resistance in the charging transformer, wiring, or semiconductor switch as these would normally be so small as to have a negligible effect on the resultant voltage and would merely serve to complicate the calculation. It has also neglected transformer secondary leakage reactance as this is a small inductance and contains no initial stored energy. Equating the time derivative of Eq. (13-6) to zero indicates that  $V_{L_p}$  is maximum when  $2\omega_0 RC = \tan \omega_0(t_1 - t_0)$ . The equation for  $V_{L_p}(\max)$  can then be written as follows:

$$\begin{aligned} V_{L_p}(\max) &= I_0 R \left[ 2 \exp\left(-\frac{\omega_0(t_1 - t_0)}{\tan \omega_0(t_1 - t_0)}\right) \cos \omega_0(t_1 - t_0) \right] \\ &= I_0 R [K_E] \end{aligned} \quad (13-7)$$

where  $(t_1 - t_0)$  = the time required after  $t_0$  to reach  $V_{L_p}(\max)$ . The values of  $K_E$ , the bracketed expression of Eq. (13-7), can be calculated as a function of  $\omega_0(t_1 - t_0)$  and are given in Table 13-4.

**Table 13-4 Values of  $K_E$  of Eq. (13-7) for different values of  $\omega_0(t_1 - t_0)$**

$\omega_0(t_1 - t_0)$	Deg.	30	35	40	45	50	55	60	65	70	75	80
	Rad.	0.533	0.611	0.698	0.785	0.873	0.960	1.047	1.134	1.222	1.309	1.396
$K_E$		0.688	0.684	0.666	0.645	0.618	0.583	0.545	0.496	0.438	0.364	0.281

From Eq. (13-7),

$$R = \frac{V_{L_p}(\max)}{I_0 K_E} \quad (13-8)$$

and from the maximization condition,

$$C = \frac{\tan \omega_0(t_1 - t_0)}{2\omega_0 R} \quad (13-9)$$

To obtain the actual values required in the transformer secondary,  $R$  must be divided by the square of the turns ratio and  $C$  multiplied by this value. Since a damped oscillatory condition was chosen to insure  $i_{L_p}$  reaching zero before the start of the next charging cycle,  $\omega_0$  should be selected so that

$$\omega_0(t_3 - t_0) + \omega_0(t_1 - t_0) \geq \pi \quad (13-10)$$

The time between pulses for the fastest repetition rate should be used for  $t_3$ . If the repetition rate is lowered,  $t_3$  will increase and  $V_{L_p}$  and the switch current will have time to reverse unless the switch is unidirectional. The silicon-controlled rectifier is essentially unidirectional except for a short turnoff or recovery time. From Eq. (13-6) it is clear that the lower the value of  $\omega_0 RC$ , the more damped will be the negative half-cycle of the waveform and, consequently, the less will be the strain on the switching device. The charging current, which was flowing through the transformer primary  $L_p$  to the PFN, is diverted to the  $RC$  network at  $t_0$ . For the conventional method with a single-winding inductor, it has the form:

$$i_{L_p} = I_0 \exp\left[-\frac{\omega_0(t - t_0)}{2\omega_0 RC}\right] \frac{\sin[\omega_0(t - t_0) + \omega_0(t_1 - t_0)]}{\sin[\omega_0(t_1 - t_0)]} \quad (13-11)$$

This current has an initial value of  $I_0$  and then decays as a damped sinusoid with its phase and magnitude determined by the value of  $\omega_0(t - t_0)$ .

From the definition of  $\omega_0$ , Eq. (13-6),  $L_p$  must be less than  $4R^2C$  for the underdamped or oscillatory condition to exist. It should also be noted that  $L_p$  must be selected in conjunction with the total PFN capacitance so that sufficient time is allowed to dissipate the energy remaining in the charging transformer. Energy remaining at the beginning of the next charging cycle will result in the charging current starting at some nonzero value. This can result in transients in the circuit and will also cause the PFN to charge at a faster rate which will affect the recovery of the main thyatron. An additional term,  $\omega L_p I_{t_3} \sin \omega t$ , must be added to Eq. (13-5) as a result of the current still flowing at  $t_3$ .

The choice of  $V_{L_p}(\max)$  is somewhat arbitrary and depends upon the difference between the maximum PFN voltage (without de- $Q$ 'ing) and the desired regulated level of PFN voltage. This does not mean that regulation will cease for voltages even higher than the design maximum but, that under certain

circumstances, some charge may pass to the PFN with a resulting increase in voltage. Referring to Fig. 13-13, it is obvious that  $V_{L_p}$  should not be allowed to rise above the regulated value of  $V_{PFN}$  for some allowable increase in  $V_{DC}$ . The normal operating magnitude of  $V_{L_p}(\text{max})$  must be somewhat less than this. A value of  $V_{L_p}(\text{max})$  equal to approximately 25% of the power supply voltage  $V_{DC}$  will provide for regulation over a considerable increase in voltage. The normal operating value of regulated PFN voltage is selected to take care of the maximum decrease expected in ac line voltage and should usually be set for a range of 3 to 5% regulation. Percentage regulation is here defined as follows:

$$\% \text{ regulation} = \frac{V_{PFN(\text{unreg})} - V_{PFN(\text{reg})}}{V_{PFN(\text{unreg})}} \times 100 \quad (13-12)$$

It should be remembered that the greater the percentage regulation, the higher the power dissipation so that some discretion is necessary in making this choice. Another point to be considered is the "dead" region resulting with very low values of regulation; that is, where the time rate of change ( $dV_{PFN}/dt$ ) approaches zero. Most comparator circuits respond in proportion to this rate of change. This region of uncertainty in de- $Q$ 'ing performance cannot be accurately defined but measurements indicate that it includes values of regulation below about 0.25%.

To complete the selection of the two required parameters, resistance and capacitance, it now remains to discuss power dissipation and energy. A comparison between the inductive voltage and current, Eqs. (13-6) and (13-11), shows that the current leads the voltage by the angle  $\omega_0(t_1 - t_0)$ . The current, therefore, reaches zero when  $\omega_0(t - t_0) + \omega_0(t_1 - t_0) = \pi$  and the energy in the inductance becomes zero at the same time. The initial energy ( $\frac{1}{2}L_p I_0^2$ ) is then stored in the capacitor, less the amount which was dissipated in the resistance. The current will try to flow in the reverse direction, with the voltage still positive across the switching device. The semiconductor switch will turn off when the current drops below a certain level, known as the holding current. A short recovery period or turnoff time is involved, but this is a matter of a few microseconds, approximately 25 in the large, high-current devices. The capacitive energy is then isolated from the inductance and is dissipated at a rate determined by the  $RC$  time constant, which is the same rate at which the damped voltage and current sinusoids were attenuated. In the actual circuit, a series  $RC$  protection against voltage spikes is placed across the switch so that a small amount of negative current continues to flow. The average power dissipated over the entire charging period is determined from the inductive energy as follows:

$$P = \frac{\frac{1}{2}L_p I_0^2}{t_3} = \frac{1}{2}(\text{PRR})L_p I_0^2 \quad (13-13)$$

where PRR is the pulse repetition rate.

The magnitude of  $I_0$ , as defined in Eq. (13-6), can also be calculated in terms of  $V_{\text{PFN}}$  and  $V_{\text{DC}}$  by combining Eqs. (13-3) and (13-5), in which case

$$I_0 = \left[ \frac{C_{\text{PFN}}}{L_p} V_{\text{PFN}} (2V_{\text{DC}} - V_{\text{PFN}}) \right]^{1/2} \quad (13-14)$$

where  $V_{\text{PFN}}$  represents the voltage at  $t_0$ , i.e., the regulated value.

So far, transformer leakage reactance has not been introduced into the analysis. The secondary leakage, which will be quite small for the low-voltage winding, has only a very minor effect on the regulation. Primary leakage inductance, on the other hand, contains energy due to the flow of charging current which is not extracted by the process of loading the secondary. The transformer should, therefore, be designed so that this leakage is as small as possible. The complexity of the circuit prevents an exact explanation of its behavior. In the first place, it was assumed that the semiconductor-charging diode was a perfect unidirectional switch and this is not exactly true—a recovery time of 10 to 15  $\mu\text{sec}$  is typical in medium-sized diodes. Second, the exact nature of the circuit is not known; only an approximate equivalent circuit can be considered. Referring to Fig. 13-13, the following simplified explanation can be given, again assuming that the charging diode ceases conduction at  $t_0$ . The primary leakage reactance will appear as a series inductance in the charging circuit, not shunted by the secondary resistance and capacitance, and having a stored energy of  $\frac{1}{2}L_L I_0^2$  joules. There is also a distributed capacitance,  $C_D$  in Fig. 13-11, from both primary and secondary to ground. This distributed capacitance on the primary side of the SLAC transformer is approximately 0.0025  $\mu\text{F}$  and can be considered in parallel with the de- $Q$ 'ing signal divider and, therefore, charged to a voltage  $V_{\text{DC}}$  at  $t_0$ . The  $R-L_p-C$  combination can be transformed approximately into a two-element series equivalent circuit and, due to the low  $Q$  of the combination, one element will be a resistor of sizable value. The leakage inductance is, therefore, still contained in a closed path which will prevent an abrupt interruption of its current flow. If transferred directly to the distributed capacitance, the inductive energy would cause a voltage rise equivalent to  $I_0(L_L/C_D)^{1/2}$ . However, the derived low- $Q$ , series  $R-L-C$  network results in a damped sinusoidal current which is initiated by an impulse function equal in magnitude to  $L_L I_0$ . The voltage which this current develops across the distributed capacitance is then superimposed on  $V_{L_p}$  of Fig. 13-13. It is considerably more damped than  $V_{L_p}$  and has a much higher frequency. Unfortunately, the exact magnitude of this voltage cannot be determined, but it could very well reach a value in excess of the regulated PFN voltage. It is, therefore, necessary to reiterate that the transformer leakage reactance should be as small as possible in order to minimize this voltage.

From the foregoing analysis, it is apparent that the entire design procedure is clouded with a certain degree of arbitrariness. Furthermore, the complexity of the equations encountered, even after simplifying assumptions are made, makes a rigorous generalized analysis of the circuit impossible. Some

insight into the problems involved, though, and a knowledge of the general approach will aid considerably in performing the circuit design.

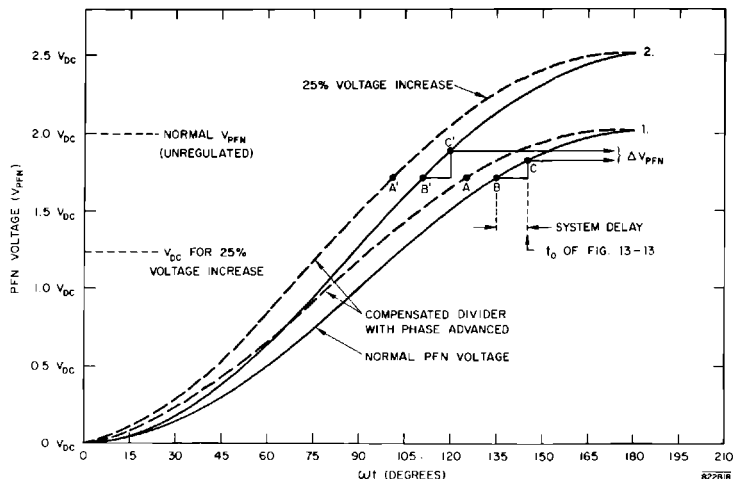
The de-Q'ing signal divider plays an important part in the accuracy obtained. Accuracy is best described as percentage error and is defined as follows:

$$\% \text{ error} = \frac{\Delta V_{\text{PFN}}(\text{reg})}{V_{\text{PFN}}(t_0)} \times 100 \tag{13-15}$$

Certain fixed delays are inherent in the system, both in the comparator and trigger circuits and in the turn-on time of the semiconductor switch. The turn-on time is typically 10  $\mu\text{sec}$  or more for high-current devices although the exact definition of full turn-on may vary somewhat. The delay in the comparator and trigger generator depends upon the circuit used and is not necessarily constant for different percentages of regulation. For a high degree of accuracy, the desired level of the attenuated  $V_{\text{PFN}}$  waveform must be compared to a very stable, highly regulated dc voltage. For small percentages of regulation, near its maximum value, the time rate of change of this voltage is very small, and the rise time of the comparator output pulse may be greater than it would be with a faster rising input signal. Nevertheless, a certain delay does exist, and assuming that it is fixed, the result of it can be seen by studying Fig. 13-14.

The solid line of waveform 1 represents a normal-amplitude PFN voltage. The command to commence regulation is given at point B, and it is assumed that the de-Q'ing signal divider is exactly compensated (zero phase shift) and the system requires about  $10^\circ$  delay, an exaggerated figure for the purpose of illustration. Therefore,  $10^\circ$  later the regulation process is complete, and the PFN voltage is set at the level represented by C. Next, consider a cycle in

Figure 13-14 Compensated de-Q'ing signal divider waveforms.



which all conditions remain the same but a 25% increase in unregulated PFN voltage occurs as represented by waveform 2. The command to regulate, now B', is given at the same voltage level although occurring earlier in time. The regulated level, again reached after a 10° delay, is set at C'. It is readily seen that this latter level represents an increase over the value attained with normal voltage, and this increment is identified as the numerator of Eq. (13-15). The denominator is taken as point C which represents  $t_0$  of Fig. 13-13.

If the waveform from the de-Q'ing signal divider is now advanced in phase by the required amount, the commands to regulate are given at points A and A' for the normal and increased PFN voltage, and the regulation occurs at points B and B'. These points now represent the same level of voltage, and the regulation is ideal; that is, the percentage error is zero. It should be noted that if the phase were advanced further, so that overcompensation existed, the regulated value of the increased voltage would be less than for the normal voltage.

To calculate the phase shift associated with the divider network, consider a divider consisting of  $n$  identical sections of  $R_1$  and  $C_1$  and an output section of  $R_2$  and  $C_2$ . This results in  $n + 2$  simultaneous integral equations and, if driven by the PFN voltage of Eq. (13-5), the solution for the output voltage across  $R_2$  is represented by the following equation. For  $V_{in} = V_{DC}(1 - \cos \omega t)$ ,

$$V_{out} = V_{DC} \frac{R_2}{nR_1 + R_2} [1 - K_1 \cos(\omega t + \theta) + K_2 e^{-t/\tau_p}] \quad (13-16)$$

where

$$\theta = \tan^{-1} \frac{\omega(\tau_1 - \tau_p)}{\omega^2 \tau_1 \tau_p + 1}$$

$$\tau_p = \frac{nR_1 R_2}{nR_1 + R_2} \left( \frac{C_1}{n} + C_2 \right) \approx R_2 C_2$$

$$\tau_1 = R_1 C_1$$

$$K_1 = \left[ \frac{\omega^2 \tau_1^2 + 1}{\omega^2 \tau_p^2 + 1} \right]^{1/2}$$

$$K_2 = \frac{\omega^2 \tau_p (\tau_1 - \tau_p)}{\omega^2 \tau_p^2 + 1}$$

An examination of this expression indicates that it reduces to the input waveform, reduced by the resistive ratio, when  $\tau_1$  equals  $\tau_p$ . For a constant phase shift, which is necessary for the greatest accuracy, the last term in the equation should be zero. Although this is not possible, the term will essentially vanish after five time constants so that the earliest reference to the waveform should be made after a time  $\geq 5\tau_p$ . In calculating  $R_2$  and  $C_2$ , consideration must be given to the input resistance and capacitance of the comparator circuit and any cable capacitance between the divider and comparator. The choice of  $R_1$  in



high-voltage circuits must take into consideration power dissipation and voltage rating, in conjunction with the desired time constant, and the number of sections required is determined by these factors. The resistors must also be noninductive with low temperature and voltage coefficients and low thermal noise. A further consideration is corona, which is associated with circuits operating above approximately 30 kV. This may make it necessary to immerse the divider in oil, as was the case with SLAC modulators. As the system time delay is never known exactly when the original modulator design is made, the practical approach is to calculate the resistors and  $C_1$  and then adjust  $C_2$  for best regulation when the circuit is tested.

The final selection to be made is the choice of semiconductor switch. This requires a knowledge of the maximum voltage to be expected across the device and the average and rms currents. Root-mean-square current is not easily determined but can be approximated closely enough for practical purposes by calculating the current for the much simpler case when the system is critically damped and  $\omega_0$  is zero. This results in

$$I_{\text{switch}}(\text{rms}) \approx I_0 \left( \frac{(\text{PRR})L_p}{1.6R} \right)^{1/2} \quad (13-17)$$

where  $R$  is the secondary resistance for the transformer-coupled circuit. Average current can be calculated by an integration of Eq. (13-11) and is accomplished by referring this current to the transformer secondary to give the following form:

$$i_{\text{switch}} = \frac{nI_0 \exp \left[ -\frac{\omega_0(t-t_0)}{2\omega_0 RC} \right] \sin[\omega_0(t-t_0) + \omega_0(t_1-t_0)]}{\sin[\omega_0(t_1-t_0)]} \quad (13-18)$$

and

$$I_{\text{switch}}(\text{AV}) = \frac{(\text{PRR})}{\omega} \int_0^{\pi - \omega_0(t_1-t_0)} i_{\text{switch}} d(\omega_0 t) \quad (13-19)$$

The upper limit of integration is obtained by solving Eq. (13-18) for the angle  $\omega_0(t_2-t_0)$  at which the switch current becomes zero. This will always be in the second quadrant and can, therefore, be written as  $\omega_0(t_2-t_0) = \pi - \omega_0(t_1-t_0)$ . The lower limit is identified as the angle  $\omega_0 t_0$  when the de- $Q$ 'ing circuit is fired and represents zero on the  $\omega_0 t$  angular scale. Inserting Eq. (13-18) in Eq. (13-19) and carrying out the integration yields

$$I_{\text{switch}}(\text{AV}) = (\text{PRR})nI_0(L_p C_{\text{PFN}})^{1/2} \left\{ \exp \left[ -\frac{\pi - \omega_0(t_1-t_0)}{\tan \omega_0(t_1-t_0)} \right] \times \sin \omega_0(t_1-t_0) + \sin 2\omega_0(t_1-t_0) \right\} \quad (13-20)$$

where  $n$  is the charging transformer turns ratio. The value of the term in braces  $\{K_f\}$  is evaluated in Table 13-5, using the same values of  $\omega_0(t_1-t_0)$  as in Table 13-4.

Table 13-5 Values of  $K_T$  of Eq. (13-20) as a function of  $\omega_0(t_1 - t_0)$ 

$\omega_0(t_1 - t_0)$	Deg.	30	35	40	45	50	55	60	65	70	75	80
Rad		0.533	0.611	0.698	0.785	0.873	0.960	1.047	1.134	1.222	1.309	1.396
$K_T$		0.871	0.955	1.020	1.066	1.100	1.118	1.124	1.122	1.109	1.091	1.066

The triggered semiconductor devices, commonly known as silicon controlled rectifiers and Trinistor controlled rectifiers, are available with current ratings up to approximately 500 A rms and voltages of 1200 V and more. The transformer turns ratio, in conjunction with the PFN voltage and current, determine the operating conditions for the switch. It should be remembered that, as a rule, the higher the current rating, the slower the turn-on time; and forcing a fast-rising current through the switch before it is fully turned on will create excessive peak power dissipation. Another precaution to be observed concerns high-voltage transients, which are prevalent in pulse modulators.\* A series  $RC$  network across the switch affords protection against such voltage spikes. If the choice between series and parallel operation of switches arises, the series connection appears to be preferable. This requires a voltage-dividing network across the two devices but ensures that the current rate-of-rise through each one is very nearly equal. Parallel operation, unless the devices are very closely matched, usually requires current-equalizing elements which are located in series with the individual switches. Furthermore, even though originally matched, it is not assured that they will remain so during their lifetime. In calculating the currents for selection of the switch, the worst-case conditions should be considered, that is, the fastest repetition rate and greatest percentage regulation that the circuit will be subjected to.

In the SLAC system, the dc reference voltage controls both the output of the ac induction regulators and the level at which PFN regulation occurs. This ensures that the percentage regulation remains about constant for any set input voltage level. The reference power supply is regulated to better than 0.01% against line and load changes and has a maximum peak ripple of 0.7 mV. This is further attenuated in the comparator to less than 0.03 mV. Regulation errors as small as 0.045% have been achieved without making a concentrated effort to reach the minimum possible. This represents a change of approximately 110 V in the 250-kV klystron pulse.

Some specific data on the de- $Q$ 'ing components used in the SLAC modulators are as follows:

CHARGING TRANSFORMER—25:1 step-down ratio.

Primary: 1.8 H inductance, 25 mH leakage inductance referred to primary, 5.7 ohms resistance.

Secondary: 0.03 ohm resistance, isolated from the primary by a grounded electrostatic shield.

\* One such voltage spike, which can be particularly harmful to the semiconductor switch, is described in the section on despiking networks.

RESISTOR—2 ohms, 8 kW. Eight 0.25-ohm, 1000-W edgewound ribbon-type resistors in series.

CAPACITOR—50  $\mu\text{F}$ , 660 V rms. Two 25  $\mu\text{F}$  ac motor-run capacitors in parallel.

SEMICONDUCTOR SWITCH—Type 2N3895 controlled rectifier, 1200 V, 175 A average, 275 A rms. Two series-connected units with voltage dividing networks across each. A series despiking network, 0.5  $\mu\text{F}$  capacitance and 25 ohm resistance, connected across the combination.

The transformer-*semiconductor* circuit offers two distinct advantages over the conventional method of regulation. The components are operated at relatively low voltage which requires much less space for insulation and the low-voltage components are generally smaller. The life of the controlled rectifier far exceeds that of gaseous tubes. An accurate projection of the lifetime cannot be made at this time; however, some of the devices at SLAC have now accumulated approximately 9000 hours operating time.

#### *Despiking network (WTT)*

The function of the despiking network is to protect the charging transformer from excessive voltage spikes and the charging diodes from excessive peak current when the main thyatron fires. The following explanation refers to the simplified schematic diagram of Fig. 13-11. The network is shown mounted in the modulator in the photograph of Fig. 13-12.

The charging transformer (or inductor) has an inherent distributed capacitance,  $C_D$ , to ground. For simplicity, this is shown as a lumped capacitance although the actual equivalent circuit is of a more complicated nature. This capacitance is charged to approximately  $V_{DC}$  when the main thyatron fires. The exact value will depend upon whether the de- $Q$ 'ing cycle is complete. If it is, then the voltage reached will be  $V_{DC}$  plus  $V_{L_p}$  as shown in Fig 13-13. In the absence of the de- $Q$ 'ing, the value reached will depend upon whether  $C_D$  in conjunction with the charging transformer and filter capacitance has had time to reach a stabilized condition after the PFN current has stopped flowing.

When the main thyatron fires and the PFN has discharged, which is approximately 3.5  $\mu\text{sec}$  later in the SLAC modulators, the PFN is left with a small positive potential and the thyatron remains in the conducting state. This is owing to the fact that the characteristic impedance of the PFN is purposely made slightly smaller than the reflected impedance of the klystron. Referring to Fig. 13-11, it is seen that a conduction path then exists from  $C_D$  through the charging diodes, the PFN, and the thyatron back to  $C_D$ . Most of the PFN inductance will be bypassed by its capacitance so that only one section of the inductance of each network is in the circuit. A rather complicated parallel path also exists through the PFN and the pulse transformer primary, although the inductance of the transformer is large enough to prevent a fast-rising current from flowing through this circuit. As the resistance of the conduction path is very low, being mostly the forward resistance

of the charging diodes, the peak current in the absence of a despiking network can reach magnitudes of many hundreds of amperes. This current, on a repetitive basis, would normally far exceed the surge current rating of the charging diodes.

Because of this current flow, the charge on  $C_D$  reverses and the voltage becomes very nearly  $-V_{DC}$ . The frequency of the waveform is a function of the equivalent series inductance and capacitance of the circuit and is approximately 500 kHz in the SLAC modulators without the despiking network. This high-frequency waveform creates excessive turn-to-turn and layer-to-layer voltages on the PFN side of the charging transformer. It is also transferred to the secondary and appears as a reverse voltage across the semiconductor switch. The ideal remedy would be a low-pass filter which offers no attenuation to the PFN charging frequency but presents very high attenuation to the high-frequency waveform. Such a filter is best approximated by a parallel  $LR$  network in series with the charging circuit as shown in Fig. 13-11. If  $L$  is some small percentage of the charging transformer primary inductance, it will have little effect on the PFN charging waveform other than to lower the frequency slightly. The resistance is selected to have a value which is much higher than the reactance of  $L$  at the charging frequency and yet lower than the reactance at the high frequency discussed above. The equivalent series network will then appear as an inductance to the charging frequency and as a resistance in series with a smaller inductance at the high frequency.

A lumped capacitance analysis of the circuit does not yield results which are useful in the design of the network. An empirical approach, used with a knowledge of the circuit behavior resulting from the added elements, is the most practical design procedure. The resistance, which serves to attenuate the high-frequency current and dissipate the energy initially stored in  $C_D$ , should be as large as possible. However, a large resistance requires a very large value of inductance as its reactance must be much greater than the resistance to allow most of the high-frequency current to flow through the resistor. From the standpoint of the PFN charging circuit and also the de- $Q$ 'ing circuit, the inductance should be as small as possible. The choice of  $L$ , then, involves attempting to satisfy these two opposing requirements. A compromise is possible because the two frequencies are generally separated by two to three decades. Experience indicates that a value of inductance in the range from 0.05 to 1.0% of the charging transformer inductance will provide a network with considerable attenuation to the high-frequency waveform. The frequency will also be lowered by the impedance of the added circuit. The resistance is selected by trial to give minimum negative voltage,  $-V_{C_D}$ , at the charging transformer.

The following data on the SLAC network illustrates the variation of  $V_{C_D}$  with resistance under operating conditions:

$R(\text{ohms})$	250	500	1000	1500	2000	2500	3000	3500	4000
$-V_{C_D}(\text{kV})$	25	20	11	8	8	8	9	11	12

For this test, the dc power supply voltage was 20 kV, the charging transformer primary inductance was 1.8 H, the transformer distributed capacitance,  $C_D$ , was 0.0025  $\mu\text{F}$ , and the despiking inductance,  $L$ , was selected to be 15 mH or 0.83% of the charging transformer inductance. It is seen that the negative voltage rises rapidly for resistances less than optimum. Also of interest is the minimum value of negative voltage obtained with four different designs of essentially the same charging transformer, each enclosed in an oil-filled case of approximately the same size. The dc power supply voltage was again 20 kV, when the following comparative data were taken:

$C_D$ ( $\mu\text{F}$ )	0.0007	0.0025	0.005	0.0185
$L$ (mH)	19.5	15	19.5	11.5
$R$ (ohms)	3000	2000	900	250
$-V_{c_D}$ (kV)	9	8	11.4	15.75

The range of distributed capacitance varies by a factor of 26 to 1, and the minimum negative voltage obtainable increases with the capacitance. This indicates that the capacitance should be kept reasonably small. The smaller capacitance will also reduce the high-frequency current that must flow through the charging diodes. Furthermore, it will reduce the stored energy, some of which is dissipated with a consequent reduction of the modulator efficiency.

#### *Switch tubes (RWB)*

Early in 1963, efforts were concentrated upon the evaluation of hydrogen thyratrons for the SLAC modulators, because spark gaps and ignitrons did not meet system requirements.

No single hydrogen thyratron which would meet all the SLAC specifications was available, so the modulators were constructed to permit the use of hydrogen thyratrons known to exist at that time, including two of the smaller tubes in a parallel PFN configuration. The two-tube system was used for initial beam tests in Sectors 1 and 2 and, in some modulators, during full beam operations for over a year with good performance.

**SPECIAL SLAC REQUIREMENTS.** The most stringent requirements imposed upon the SLAC thyratron centered around the anode delay time, variation (variation in switching time from minimum voltage and pulse rate to maximum voltage and pulse rate), instantaneous starting at full voltage, and long mean time between faults.

The variation in delay time through the SLAC modulators is an important parameter because it is desirable to utilize as much of the flat-top portion of the pulse as possible for beam acceleration.

The instantaneous start requirement is necessary because it would be impracticable to spend extra time varying operating voltages to get modulators back on whenever a fault occurred.

Table 13-6 Hydrogen thyratron specifications

Peak anode forward voltage ( $e_{pf}$ )	46 kV (max)
Peak anode inverse voltage ( $e_{pi}$ )	5 kV (max)
Pulse duration ( $T_p$ )	4 $\mu$ sec (max)
Peak anode current ( $i_b$ )	4000 A (max)
Average anode current ( $I_b$ )	5 A (max)
Rms anode current ( $i_p$ )	140 A (max)
Anode delay time ( $T_{ad}$ )	0.4 $\mu$ sec (max)
Anode delay time jitter ( $T_j$ )	0.01 $\mu$ sec (max)
Anode delay time drift ( $\Delta T_{ad}$ )	0.04 $\mu$ sec (max)
Anode delay time variation ( $\Delta T_{adv}$ )	0.15 $\mu$ sec (max)
Anode dissipation factor ( $P_b$ )	$70 \times 10^9$ (max)
Pulse repetition rate (PRR)	60 to 360 pulses/sec
Number of kickouts	4 (max) in 96 hours
Operating life (objective)	10,000 high-voltage hours

The long mean time to fault is required for beam stability. There are 245 modulators in the accelerator and even at four faults per 96 hours, which is the maximum fault rate specified, the mean time to fault for all the tubes in the accelerator would be approximately 6 min.

The principal specifications for the hydrogen thyratrons are shown in Table 13-6.

In order to meet the SLAC specifications the manufacturers incorporated a pretrigger electrode and modified the grid and baffle configurations for optimum switching time and low kickout rate.

**PRETRIGGER ELECTRODE.** The maximum anode delay in the hydrogen thyratron is largely determined by the time it takes the plasma in the relatively large cathode region to build up to a critical density in the control grid aperture region. When this point is reached, the tube begins to conduct. In order to reduce the ionization build-up time in the cathode region, a pretrigger electrode was installed between the cathode and the control grid (see Fig. 13-15). This electrode is connected to the trigger transformer through a 250-ohm resistor. The control grid is connected to the trigger transformer through an LC filter network. There is a delay through this network of approximately 0.1  $\mu$ sec which allows current to flow to the pretrigger electrode and partially ionize the cathode region prior to application of the grid trigger. This mode of operation reduces the cathode ionization time from approximately 600 to 230 nsec and reduces the cathode ionization time variation from a nominal 350 to 100 nsec.

**KEEP-ALIVE OPERATION.** During the development phase, experiments were done with a constant dc voltage applied to the pretrigger electrode. The effect of the keep-alive voltage was to reduce the ionization time in the cathode

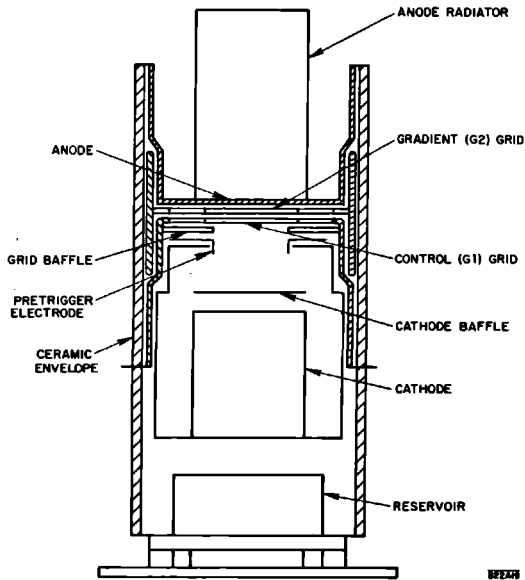
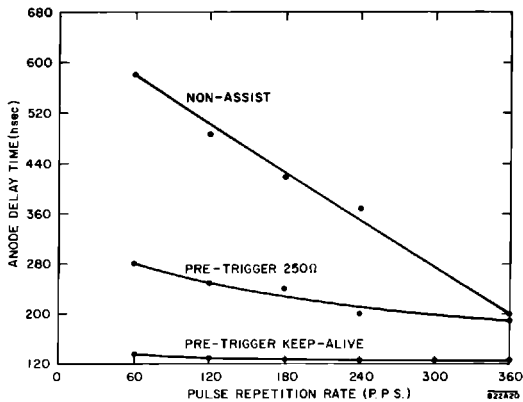


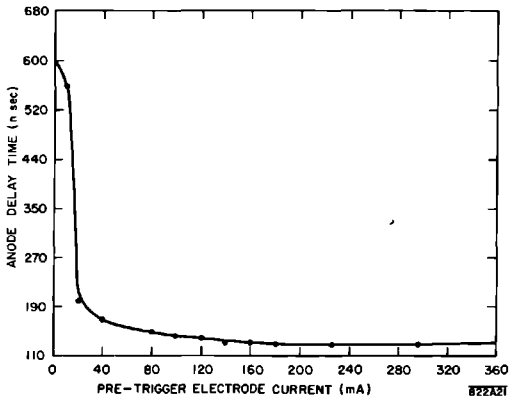
Figure 13-15 Typical SLAC hydrogen thyratron, showing grid structure and pretrigger electrode.

1 to approximately 80 nsec and the cathode ionization time variation to an 10 nsec. The effect of the three trigger modes on anode delay time can be seen in Fig. 13-16.

As can be seen in Fig. 13-17, the anode delay time is essentially stable at 180 mA of keep-alive current on a new tube and is stable above 200 mA tubes with 7000 hours, or more, of operation. About 2A through this

Figure 13-16 Anode delay time vs repetition rate for three trigger modes.





**Figure 13-17** Anode delay time vs pretrigger electrode current.

electrode are required to fire the tube. It was decided to run the SLAC thyatron at a keep-alive current of 350 mA.

An additional benefit from operation of these tubes in the keep-alive mode was a marked increase in operating life. It is believed that a 3–5 times increase might be expected for a tube in this power class.

In order to help the manufacturers meet specifications, the effects of varying element spacings were studied at SLAC, and it was possible to correlate the delay times attributed to the different electrodes in the thyatron with tube dimensions. Several tubes with varying dimensions were built so that these effects could be studied. Manufacturing tolerances were minimized through direct measurements of interelectrode spacing from x-ray prints using high-energy, cobalt-60, x-ray techniques. It was noted for instance<sup>2</sup> that the spacing between the control grid  $G_1$  and the cathode baffle was most critical (being the longest portion of the discharge path). The separation also varied critically with the focusing effect of the cathode aperture. A change of 0.020 in. (10%) in some cases accounted for delay changes of 170 nsec through this space. It was found that a spacing between 0.170 and 0.200 in. for a given cathode aperture was satisfactory for one type tube. The effect of  $G_1$  to  $G_2$  (gradient grid) spacing was studied, and a spacing of 0.125 to 0.135 in. was found to be optimum. Greater spacings produced greater delay time in  $G_1$  to  $G_2$  transfer which was probably due to the reduced field intensity or penetration in the  $G_1$  slot. Closer spacing than 0.120 in. produced excessive kickouts. The anode to  $G_2$  spacing was optimized between 0.115 and 0.120 in. Larger spacings produced excessive time delay. Spacings less than 0.115 in. caused arcing and kickouts. Of course, the dimensions vary for other tube types, but the effects are the same.

**CIRCUIT CONSIDERATIONS AFFECTING THYRATRON OPERATION.** In order to achieve good performance and long life, it was necessary to tailor the modulator circuit and operating conditions to the tube. Two important thyatron



characteristics affecting the modulator design are recovery time and anode delay time stability. Also, the PFN charging circuit affects switch tube recovery. As slow a charging rate as possible was allowed, consistent with ability to de-Q the charging transformer at the highest repetition rate. Even so, the charging current does not start at zero, which has the effect of reducing recovery time from 300 to 225  $\mu\text{sec}$ .

The end-of-line clipper protects the switch tube and modulator from high inverse voltages due to load arcing and also has a pronounced effect on the normal inverse recovery voltage.

The thyatron trigger affects the anode delay time. A high amplitude trigger from a low impedance source reduces anode delay time. It was found that about 2000 V from a 25-ohm source was adequate.

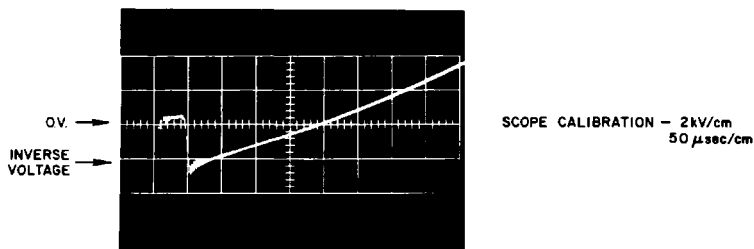
Stored energy in the shunt inductance and capacitance of the pulse transformer affects the switch tube recovery and dissipation. The resulting currents during recovery time tend to force re-conduction of the thyatron after the main pulse. Energy stored in the leakage inductance of the pulse transformer is another principal source of postpulse current. It causes "spikes" on the anode voltage waveform during the recovery period and results in tube faults.

The impedance match between the PFN and load is important for proper operation of the thyatron. One of the more common methods of obtaining inverse voltage is the "negative mismatch" mode of operation. In this mode, the load impedance is less than the PFN impedance, causing a reflected negative voltage to appear on the anode of the switch tube immediately after the pulse. The disadvantages of this are (1) increased anode dissipation due to ion bombardment as a result of negative voltage on the anode immediately after the main pulse, while the tube is still in a heavily ionized state; (2) high spikes on the anode during recovery time, as a result of the energy stored in the pulse-transformer leakage inductance; (3) the pulse-transformer stored energy cannot be transferred to the PFN in the negative mode and must be dissipated in an additional circuit (primary pulse-transformer clipper) if klystron backswing voltage and pulse-transformer losses are to be minimized.

A second method of obtaining inverse voltage (the one used at Stanford) is the "positive" mismatch mode of operation, where the load impedance is higher than the PFN impedance, and some positive voltage is left on the PFN network after the main pulse.

The energy stored in the pulse-transformer shunt inductance is transferred through the thyatron to the PFN in a time period determined by the pulse-transformer shunt inductance and the total PFN capacitance. In the SLAC modulator the thyatron is kept conducting for approximately 50  $\mu\text{sec}$  after the end of the main pulse. This is followed by the application to the anode of a 4-kV negative pulse which decays in about 175  $\mu\text{sec}$ . (See Fig. 13-18).

The thyatron in this mode performs the function of a pulse-transformer primary clipper, but since the pulse-transformer stored energy adds to the next charging cycle instead of being dissipated, the overall modulator efficiency is improved. Other advantages of positive mismatch mode operation



**Figure 13-18** Typical postpulse thyatron anode voltage waveform.

are reduction in anode spike amplitude and a marked increase in time between tube faults. In some tube types a 10:1 reduction in the number of tube faults for a given period has been observed.

**RANGING.** In order to obtain stable high-voltage operation and long life, the switch tubes are operated at optimum hydrogen pressure for that particular tube.

Lower pressures improve high-voltage holdoff characteristics but at the same time increase tube voltage drop and cause cathode stripping or depletion due to excessive ion bombardment and excessive anode temperatures. High pressure, on the other hand, decreases tube dissipation but results in excessive fault rates.

The pressure in the hydrogen thyratrons is controlled by varying the heater power to titanium reservoirs. The SLAC thyratrons have a typical reservoir range of  $\pm 10\%$  ( $\pm 0.4$  V) from the center of the range. It is necessary to check the center point at 500-hour intervals to insure optimum life because the reservoir center point may shift due to hydrogen cleanup. This checking and adjustment procedure is known as "ranging." The shift in reservoir set point cannot be predicted and in some instances there has been no significant shift. Figure 13-19 is a plot of reservoir center range versus age for three typical tubes at full SLAC power. Ranging is a time-consuming maintenance problem because 245 thyratrons are involved and it takes about 15 min to range each one.

Two methods have been investigated. The first method is the traditional hot ranging technique whereby the reservoir voltage is lowered by 0.1-V intervals until grid hash or commutation spikes are observed on the grid waveform which indicates the low pressure limit. The reservoir is then raised in 0.1-V intervals until the thyatron faults, which is the high pressure limit. Halfway between the extremes is the reservoir center point or optimum hydrogen pressure. The disadvantage of this method is that it is time consuming.

A second method developed at SLAC is the thyatron RF noise detector. There are numerous frequencies generated within the tube which change in amplitude with tube pressure and which are independent of the external

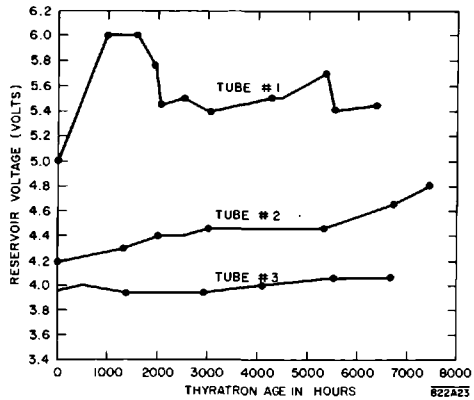
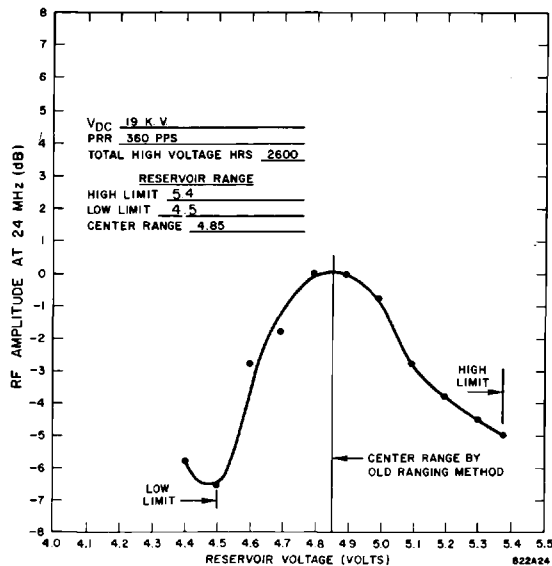


Figure 13-19 Typical reservoir center range vs thyatron age in hours.

circuit. The useful frequency for pressure setting in the SLAC thyatron occurs at 24 MHz. At this frequency the RF power peaks at the center of the pressure range and drops off about 4 dB at the range limits. Figure 13-20 shows a plot of RF pickup at 24 MHz versus reservoir voltage for a typical SLAC thyatron. The principal advantages of this system are greater speed and accuracy in ranging. The optimum pressure can be determined accurately in less than one-third the time required by the old method.

Figure 13-20 Plot of RF amplitude at 24 MHz vs reservoir voltage.



**THYRATRON LIFE.** At this writing insufficient life information is available to estimate accurately the life of the hydrogen thyatron tubes in the accelerator. Some life-test tubes have been run 7000 hours at full power and some have been run 5000 hours, but it is expected that the average life of the first generation of tubes will be 3000 to 4000 hours. It is hoped to achieve the design objective of 10,000 hours within three tube generations when the failure modes are identified and the necessary modifications are incorporated.

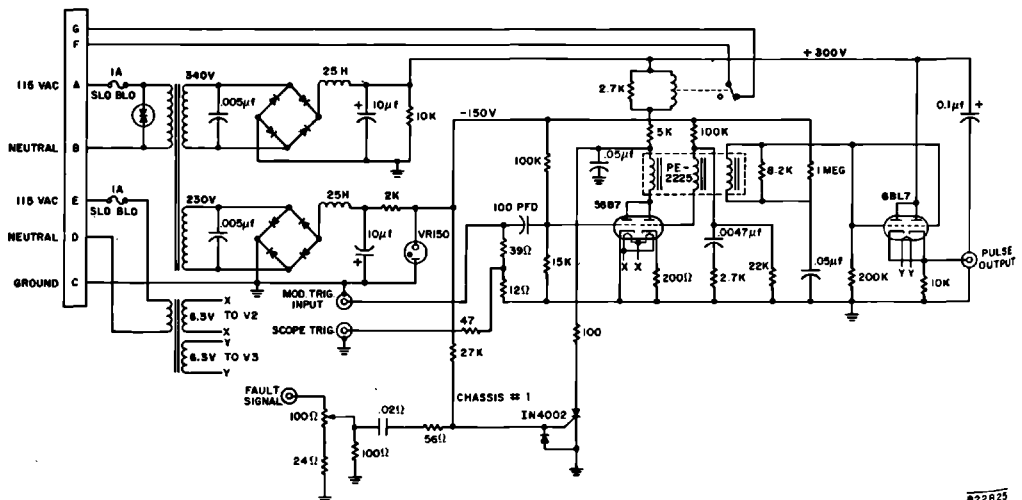
### *Thyratron trigger system (RWB)*

The trigger circuit incorporated in the modulator to furnish a grid trigger pulse to the high-power hydrogen thyatron switch tube consists of two separate units identified as trigger chassis Nos. 1 and 2. Schematic diagrams of these units are shown in Figs. 13-21 and 13-22.

Trigger chassis No. 1 consists of two power supplies, a driven blocking oscillator, a cathode follower output stage, and a fault interlock and gating circuit. This unit accepts the input pulse from the sector trigger generator and amplifies it to a level sufficient to drive trigger chassis No. 2. The input pulse has an amplitude of approximately 50 V, a duration of 2  $\mu$ sec, and a rise time of 50 nsec. The output pulse is approximately 200 V, has a duration of 3  $\mu$ sec, and a rise time of 50 nsec.

Trigger chassis No. 2 is a scaled-down version of the modulator's high-power pulse circuit. Specifically, the circuit consists of a 5-kV dc supply, a charging choke and diode, a PFN, a pulse transformer, a hydrogen thyatron switch tube, and other supporting components. The circuit functions the same

**Figure 13-21** Thyatron trigger chassis No. 1.



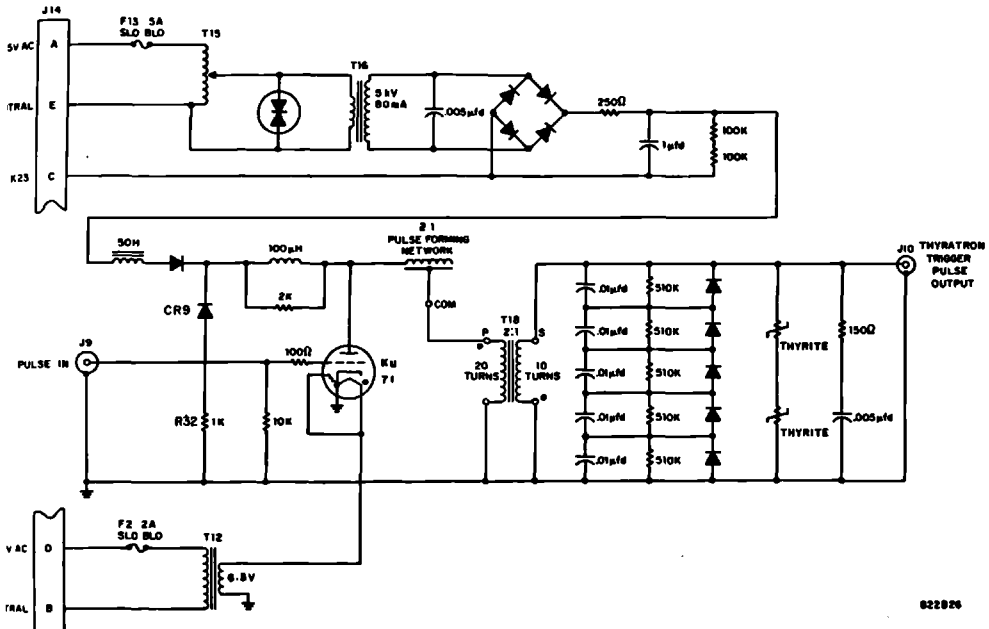


Figure 13-22 Thyatron trigger chassis No. 2.

as a line-type modulator. The 5 kV from the power supply is increased to approximately 8 kV across the PFN capacitors by dc resonance charging. When the driver hydrogen thyatron switch tube is triggered by the pulse from trigger chassis No. 1, the PFN capacitor's stored energy is discharged through the primary of the pulse transformer, the switch tube, and the PFN inductors. Half of the voltage on the PFN capacitors is dropped across the pulse transformer to produce the output pulse and half appears across the PFN when working into a matched load. However, this circuit works into a high impedance load until the main thyatron fires, at which time the load impedance drops to a low value, so most of the PFN charge is reflected back to the PFN where it is dissipated in the inverse diode circuit consisting of CR 9 and R 32.

When the main switch tube fires, its control grid assumes a potential dependent on the voltage gradient from plate to cathode and its relative position between these two elements. During tube commutation this potential may vary from 2 kV for normal operation to 10 kV during load faults. To safeguard the driver from possible damage due to these high-voltage transients, protective circuits consisting of a low-pass  $LC$  filter, spark gap, and a Thyrite assembly were added on the secondary side of the pulse transformer.

The output pulse has a maximum voltage level of 4 kV when the main thyatron switch tube is nonconducting and supplies about 200 A when the switch tube is in conduction. Its pulse width is 2  $\mu$ sec and rise time 0.2  $\mu$ sec (maximum).

### *Pulse transformer (RMR)*

The pulse transformer is the link between the modulator and the main klystron amplifier (see Fig. 13-23). Therefore, its band pass and power handling characteristics have to be such that the modulator output pulse will be transmitted with minimum distortion and attenuation.

With this requirement in mind, the operating specifications shown in Table 13-7 were developed for the pulse transformer.

In order to obtain a transformer of minimum volume and weight, the manufacturer made use of a reset core. In this design, the core is held near negative saturation during the interpulse interval by a steady, direct bias current of approximately 12 A. This current is supplied to the primary of the pulse transformer through a 2.5-mH inductor. The inductor is required to isolate the bias power supply from the high-voltage primary pulse. This scheme permits a flux swing of 17.5 kG at 250 kV and 3.5- $\mu$ sec effective pulse width.

The core of the pulse transformer is made up of 3 smaller "subcores" strapped together. Each subcore is wound from 0.002-in. thick, grain-oriented silicon steel ribbon,  $1\frac{5}{8}$  in. wide. The buildup of the winding is  $2\frac{3}{8}$  in. The window opening in the core is  $7\frac{1}{8}$  in. long and  $3\frac{3}{4}$  in. wide.

The primary winding of the pulse transformer consists of six turns of five No. 16 AWG conductors in parallel on each leg of the core. The two primary

**Figure 13-23** Klystron and pulse-transformer tank.

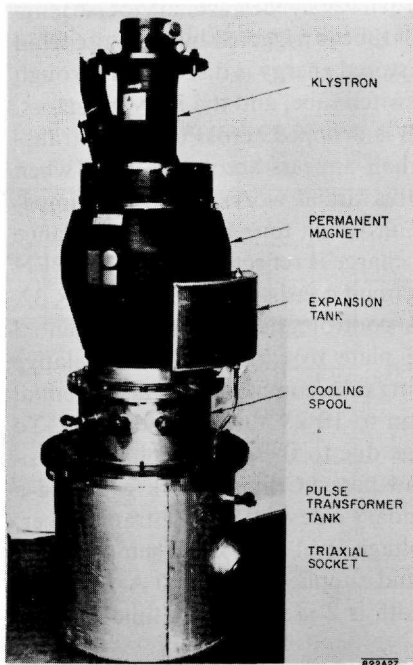


Table 13-7 Pulse transformer specifications

<i>Input</i>		<i>Output</i>	
Peak voltage	20.8 kV (negative)	Load	Perveance $2 \times 10^{-6} \pm 5\%$ (klystron)
Peak current	3000 A (nominal)	Load shunt capacity	$90 \pm 20\%$ pF
Rise time (5–95%)	0.5 $\mu$ sec (max)	Peak voltage	250 kV (negative)
Pulse duration	3.7 $\mu$ sec (max at 70% amplitude)	Peak current	250 A (nominal)
Fall time (95–5%)	0.5% $\mu$ sec (max)	Rise time (5–95%)	0.7 $\mu$ sec (max)
Flat-top duration	2.8 $\mu$ sec (min)	Flat-top duration	2.5 $\mu$ sec (min)
Pulse repetition rate	360 pulses/sec (max)	Pulse top ripple	$\pm 0.5\%$ (max)
Pulse top ripple	$\pm 0.3\%$ (max)	Droop of flat top	2% (max) with isolation inductor
Turns ratio	1:12 (exact)	Fall time (95–5%)	1.2 $\mu$ sec (max)
		Pulse undershoot	15% (max)
		Pulse return swing	10% (max)

windings are connected in parallel. There are two secondary windings of seventy-two turns each, connected in parallel. One secondary is wound on each leg. The secondary conductors are No. 18 AWG.

In a step-up pulse transformer, pulse rise time is proportional to the square root of the product of leakage inductance and shunt capacitance (transformer distributed plus load strays). The leakage inductance in the SLAC pulse transformer was minimized by employing a “constant gradient”<sup>3</sup> or tapered secondary winding. (See Fig. 13-24). In this type of winding, the volume enclosed by the leakage flux (and hence the leakage inductance) is approximately one-half of what it would be if the coils were of conventional, parallel-sided, concentric construction. The leakage inductance was further reduced by winding a complete primary and secondary on each leg of the core and then connecting them in parallel<sup>1</sup> as noted above. This technique also simplified the problem of feeding low-voltage ac power to the klystron filament transformer, since the pulse-transformer secondary windings provided the necessary high-voltage pulse isolation. The pulse-transformer equivalent circuit parameters are summarized in Fig. 13-25. With the realization that few if any transformer manufacturers had facilities to check the wave-shape characteristics of this transformer under full voltage operating conditions, a low-voltage, pulse-shape acceptance test was specified for rise time and pulse top ripple. The theoretical basis for this type of test has been well established.<sup>4</sup> Correlation between low-voltage pulse tests and high-voltage operation was excellent.

The klystron filament power is supplied by a 325-VA toroidal transformer housed within the klystron socket. The transformer is the “auto” type and

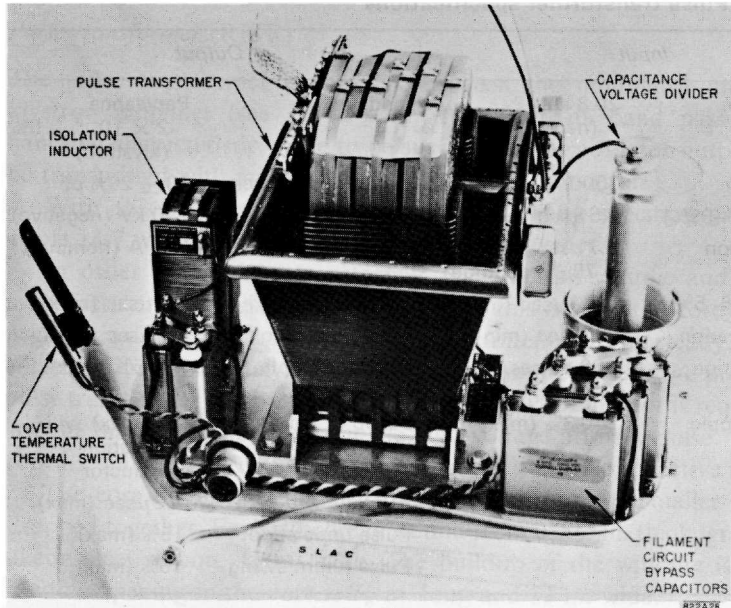


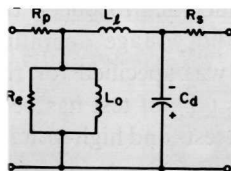
Figure 13-24 Pulse transformer and associated components.

floats at high voltage. There was no room in the transformer tank for a low-capacitance, filament isolation transformer of the type conventionally used in cathode-modulated power tube circuits. The filament transformer can be seen on top of the pulse transformer in Fig. 13-26.

The capacitance voltage divider with a division ratio of 5000:1 allows direct viewing of the klystron cathode pulse. The divider, which can be seen in Figs. 13-24 and 13-26, is coaxial and has a fully shielded pickup ring. The characteristics and advantages of this type divider are discussed in References 5 and 6.

For ease of assembly and servicing, the pulse transformer, pulse isolation inductor, capacity voltage divider, and filament circuit bypass capacitors are

Figure 13-25 Equivalent circuit of the pulse transformer.



ALL VALUES ARE REFERRED TO  
HIGH VOLTAGE SIDE

$R_p = 0.6\Omega$  PRIMARY DC RESISTANCE  
 $R_e = 58K\Omega$  EQUIVALENT CORE LOSS  
 $L_o = 110$  mH TRANSFORMER OPEN  
 CIRCUIT INDUCTANCE  
 $L_l = 224\ \mu$ H LEAKAGE INDUCTANCE  
 $C_d = 100$  pF DISTRIBUTED CAPACITANCE  
 $R_s = 1.05\Omega$  SECONDARY DC RESISTANCE  
 (SUM OF BOTH WINDINGS)



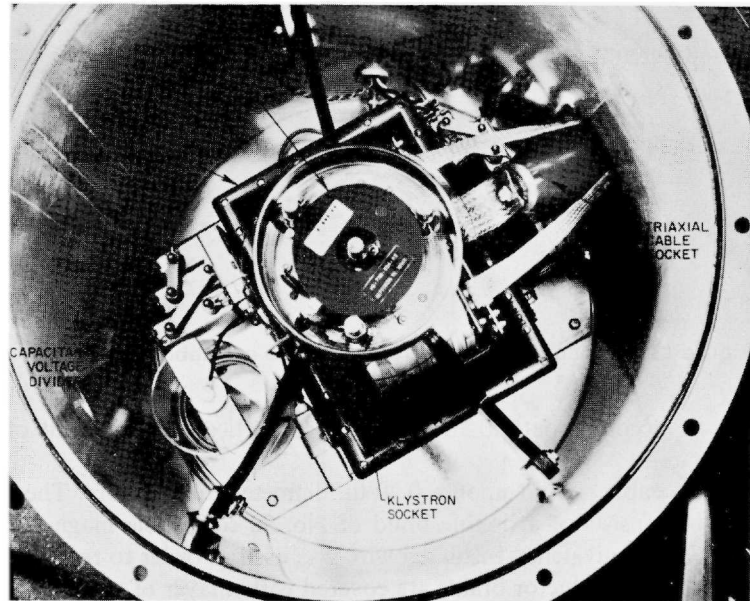
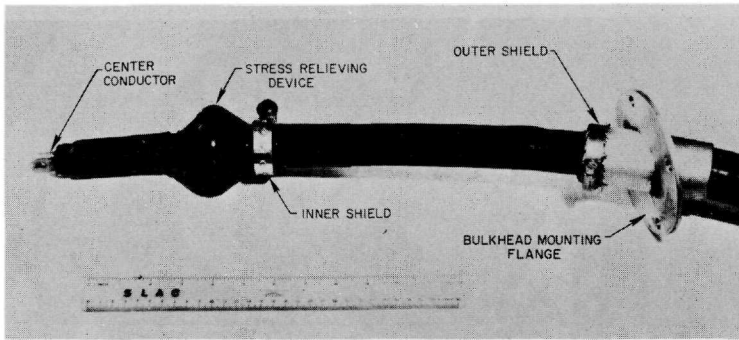


Figure 13-26 Pulse transformer tank, top view.

mounted on an aluminum base plate (Fig. 13-24). This assembly is housed in a 22-in. diameter  $\times$  22-in. deep aluminum tank. The klystron socket assembly is supported on epoxy insulating arms from the sides of the tank (Fig. 13-26). The klystron tube is supported on a flanged double-walled stainless steel cooling spool which is bolted to the top flange of the tank. Cooling for the insulating mineral oil, with which the entire assembly is impregnated, is provided by the klystron collector cooling water which circulates between the double walls of the cooling spool. The maximum temperature rise of the oil is  $42^{\circ}\text{C}$  under full power operating conditions (250 kV, 360 pulses/sec), maximum cooling water inlet temperature ( $35^{\circ}\text{C}$ ), and maximum ambient air temperature ( $43.5^{\circ}\text{C}$ ). This temperature rise causes an increase in oil volume of approximately 230 in.<sup>3</sup>. The increase is accommodated by an external expansion tank bolted to the klystron mounting flange. The pulse transformer tank and its contents are protected from overtemperature operation by a thermal switch (extreme left of Fig. 13-24) set to open at  $85^{\circ}\text{C}$ . The thermal switch is part of the modulator interlock chain. The klystron pulse tank assembly is shown in Fig. 13-23.

#### *Triaxial pulse cable assembly (RMR)*

The pulse power from the main modulator is delivered to the pulse transformer tank by means of a high-power, triaxial, pulse cable assembly. This assembly is required to be sufficiently flexible to allow easy coupling and uncoupling



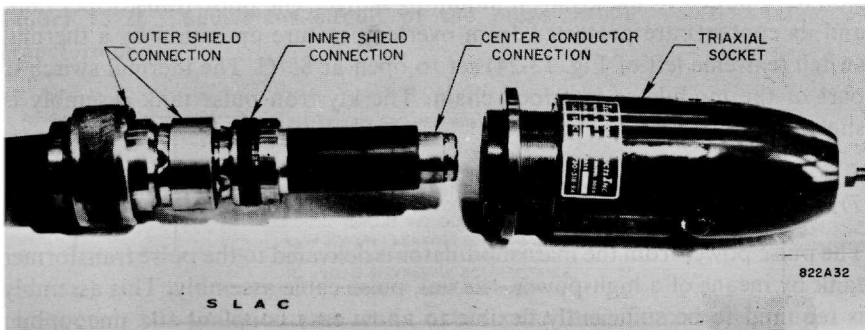
**Figure 13-27 Modulator end of pulse cable assembly.**

and to accommodate a 2 ft variation in vertical displacement of the pulse tank.

The cable is built upon a 0.70-in. diameter, rubber core. The center conductor consists of a double braid of No. 30 solderable magnet wire (No. 4 AWG dc equivalent). Insulated wire was used in order to reduce skin effects. The center conductor braids are covered with a layer of semiconducting tape, and then served with layers of oiled polyethylene tapes to build the major insulation to a thickness of 0.050 in. The second braid, also No. 4 AWG dc equivalent, provides the pulse current return path. The outer braid is the RFI shield braid and assures that the modulator cabinet and pulse-transformer tank remain at the same potential.

The pulse cable assembly consists of an air end termination and a stress-relieving device (Fig. 13-27) which are installed in the modulator, and an oil end termination (Fig. 13-28). The oil end termination consists of two parts: a socket which is installed in the pulse tank and a male plug which is built up on the end of the cable. The socket contains the stress-relieving device for the oil end of the cable assembly.

**Figure 13-28 Pulse-transformer tank end of pulse cable assembly.**



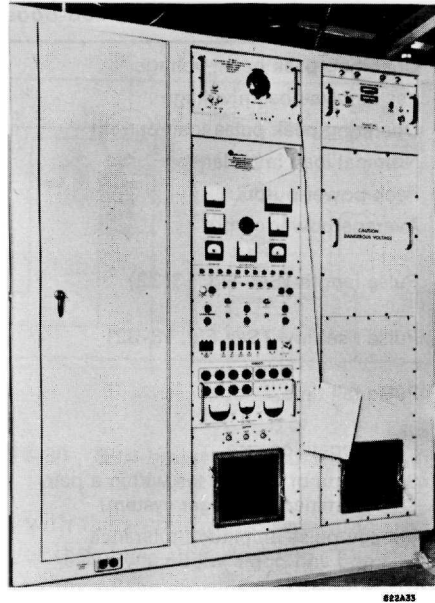


Figure 13-29 Sub-booster modulator.

## 13-2 Sub-booster modulator (FTV)

### *General description*

The sub-booster modulator, shown in Fig. 13-29, is part of the drive system of the accelerator. In conjunction with a sub-booster klystron, its main function is to amplify a 2856-MHz RF signal from approximately 60 mW to a minimum of 60 kW with strict requirements relating to rise and fall times and amplitude tolerances.

The stringent specifications established for the beam voltage pulse are of primary importance because the pulse shape determines the rise and fall time of the RF output pulse, and its phase shift, which ultimately has a large effect upon the energy spectrum of the electron beam.

One unit per sector (total 30) supplies the RF power through a coaxial subdrive line to the eight 24-MW klystrons of a sector.

The klystron tube used in the sub-booster modulator is a 60-kW, S-band, fixed tuned, pulsed amplifier with coaxial input and output connectors. For more details see Chapter 9.

The characteristics of the sub-booster modulator are given in Table 13-8.

### *The sub-booster modulator circuit*

The sub-booster modulator is of the hard tube type.<sup>1</sup> The plates of the switch tubes are connected to a storage capacitor  $C_n$  and the filaments are at

**Table 13-8 Specifications of sub-booster modulator**

Operating peak beam voltage	26 to 28 kV (negative)
Peak inverse beam voltage	1 kV (max)
Operating peak pulse load current	7–12 A
Nominal load impedance	2333–3328 ohms
Peak power output	336 kW
Average power output	660 W for 2.5- $\mu$ sec pulse length 890 W for 3.5- $\mu$ sec pulse length
Pulse length (See Fig. 13-32)	2.5 $\pm$ 0.020 $\mu$ sec 3.5 $\pm$ 0.1 $\mu$ sec
Pulse rise time (See Fig. 13-32)	0.2 $\mu$ sec (max) (10–100%) 0.1 $\mu$ sec(max) (75–100%)
Pulse fall time	1.5 $\mu$ sec (max) (100–10%) 0.15 $\mu$ sec (max) (100–75%)
Pulse repetition rate	360 pulse-pairs/sec
Separation of two pulses within a pair (determined by trigger system)	20–100 $\mu$ sec
Voltage pulse amplitude tolerance	
Droop and ripple within any pulse or pulse pair	0.08% (max)
Amplitude variation and drift	0.04% (max)/5 min 0.08% (max)/1 hour 0.16% (max)/24 hours 0.32% (max)/168 hours
Pulse delay time	0.4 $\mu$ sec (max)
Pulse delay time jitter	$\pm$ 10 nsec (max)
Pulse delay time drift	15 nsec (max)/hour 60 nsec (max)/24 hours

ground potential (see Fig. 13-30). The other side of the capacitor is connected to the klystron load.

A resistor is used as an isolating element between the pulser circuit and its associated high-voltage power supply.

When the grids of the switch tubes are driven positive and the tubes start to conduct, a large proportion of the voltage across the capacitor  $C_n$  appears across the klystron, since it is the highest impedance in the series circuit, consisting of the switch tubes, the storage capacitor  $C_n$ , and the klystron.

One of the major design considerations was the requirement for an extremely flat pulse to minimize the phase shift in the RF output of the klystron tube. Any change in the amplitude of the beam voltage pulse applied across the klystron causes phase shift in the RF output pulse of the klystron. For the particular klystron used in the sub-booster, a change in beam voltage amplitude of approximately 26 V (0.1%) corresponds to a phase shift of 1°. This is the maximum allowed for all possible deficiencies, such as ringing, droop, and overshoot. Radio-frequency phase measurements were made on all sub-boosters to check that they met these stringent requirements.

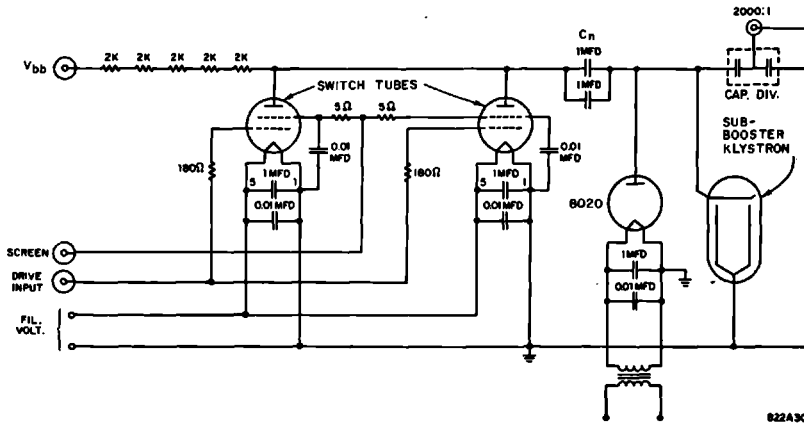


Figure 13-30 Sub-booster modulator circuit.

The requirement of a pair of pulses, with the second pulse separated from the first by 20 to 100  $\mu\text{sec}$ , also aggravates the phase shift problem. The short interpulse period relative to the charging time of the storage capacitor results in an amplitude difference between the two pulses. The magnitude of this difference and the amount of droop in each pulse can be minimized by selecting a large value for  $C_n$ . This will be evident by the example given below.

From the simple circuit diagram of Fig. 13-31, it may be deduced that the voltage across the klystron changes according to the formula,

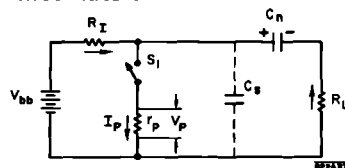
$$V_L = V_{bb} \cdot \exp\left\{-\left[\frac{\tau}{(R_L + r_p)C_n}\right]\right\} - V_p \quad (13-21)$$

where

- $V_{bb}$  = the initial voltage across  $C_n$
- $\tau$  = the duration of the pulse
- $R_L$  = the load resistance (klystron)
- $V_p = I_p \times r_p$  = the voltage drop across the switch tubes
- $r_p$  = the effective resistance of the switch tubes.

If the pulse width  $\tau \ll (R_L + r_p)C_n$ , only a small fraction of the energy in  $C_n$  is discharged. The change in the amplitude of the beam voltage pulse is

Figure 13-31 Simplified circuit diagram of sub-booster modulator.



called "droop,"  $\Delta V_L$ , and its magnitude can be reduced by making the storage capacitor  $C_n$  larger for a given value of pulse current and pulse width. This follows from the relation,

$$\Delta V_L = \frac{I_L}{C_n} \cdot \tau \quad (13-22)$$

which is valid if  $\tau \ll (R_L + r_p)C_n$ . A large value for  $C_n$  reduces the difference in amplitude between the two pulses of a pair, because the delay time of 20 to 100  $\mu\text{sec}$  is very small compared to the recharge  $RC$  time constant of the modulator.

These calculations on storage capacitor discharge during a pulse are made assuming a resistive load. For all practical purposes, the results can be applied to the use of biased diode-type loads such as the klystron.

A disadvantage of the large physical size of the storage capacitor is the stray capacitance to ground  $C_s$ , of the capacitor case (see Fig. 13-31). This stray capacitance appears as a shunt capacitance across the klystron load. A major effort has been made to keep the total stray capacitance  $C_s$  to a minimum, in order to obtain the required rise time. A list of the capacitances to ground for various circuit components is given in Table 13-9. The total stray capacitance, including connecting straps, is approximately 160 pF.

The stray capacitance of the circuit determines to a large extent the peak current the switch tubes have to supply if a fast pulse rise time is a prerequisite. This current is in addition to the load current and the current drawn by the isolating resistors between power supply and pulser during the pulse.

The peak current required to discharge the stray capacitance must satisfy the formula,

$$I_c = C_s \cdot \frac{\Delta V_B}{\Delta t}$$

where

$C_s$  = the stray capacitance

$V_B$  = the beam voltage

$\Delta t$  = the rise time

**Table 13-9 Capacitances to ground for various circuit components**

<i>Component</i>	<i>Capacitance (pF)</i>
Klystron tube input capacitance	16
Filament transformer	16
Pulse voltage divider	5
Current viewing transformer	5
Recharge diode	5
Charging resistor assembly	13
Switch tubes, output capacitance	32
Storage capacitor case to ground	60

For the sub-booster modulator under consideration,

$$V_B = 28 \text{ kV}$$

$$C_s = 160 \text{ pF}$$

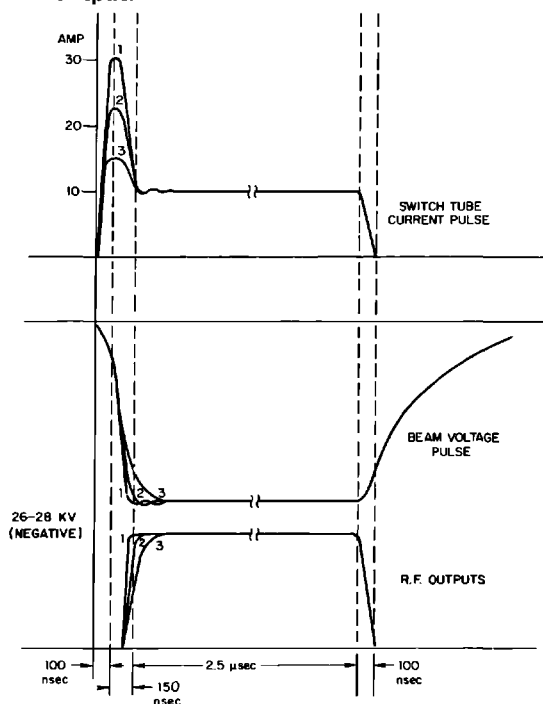
$$\Delta t = 200 \text{ nsec}$$

$$I_c = 160 \times 10^{-12} \cdot \frac{28 \times 10^3}{200 \times 10^{-9}} = 22.4 \text{ A}$$

The current drain in the 10-kohm isolating resistors during the pulse is 2.8 A. (See Fig. 13-30.) The sub-booster modulator requires approximately 30–32 A for a rise time of 180 to 200 nsec (10–100%). In this case, it is clearly shown that the peak switch tube current in a fast rise time pulser will be several times the value of the load current (7–12 A).

It can also be shown that if the grid drive pulse to the switch tubes has a finite rise time (in the present case 0–800 V in 100 nsec), the switch tube current will increase linearly during part of the rise time and then decrease when the beam voltage reaches its minimum value, or “bottoms out.” The current during the remainder of the pulse duration is determined by the klystron and the current lost in the isolating resistors. (See Fig. 13-32). For this to be true,

**Figure 13-32** Effect of peak current capability of switch tubes on rise time of beam voltage and RF output.



the cathodes of the switch tubes must be capable of supplying this large peak current.

The peak current capability of the switch tubes depends on the cathode or filament emission, most often expressed in milliamperes per filament watt. A drop in this peak current emission capability, due to decarburization of the thoriated tungsten filaments, for example, will result in increased rise time.

A drop in the peak current capability will also cause a corresponding decrease in the width of the flat-top portion of the pulse and a sharp increase in the rise time of the RF output pulse, due to the  $\frac{1}{2}$  power law behavior which the klystron exhibits (see Fig. 13-32).

To eliminate any trace of ac ripple in the RF output pulse, the filaments of the switch tubes and the klystron are supplied with dc power.

#### *The fall time of the beam voltage pulse*

The value of the stray capacitance also has an important effect on the pulse fall time for the following reason.

Referring to Fig. 13-31, it can be seen that upon opening switch  $S_1$  the stray capacitance charges through  $R_f$  in parallel with  $R_L$ . ( $C_n$  can be considered a short circuit during this time because its voltage does not change appreciably during the fall time.)

The only way to improve the fall time in an arrangement where the klystron load is one determinant and the stray capacitance has been kept to a bare minimum value, is to reduce the resistance value of the isolating element between the pulse circuitry and its power supply. However, a lower resistance value means an increase in the current lost in this element during the pulse, and it necessitates an increase in peak current requirements for the switch tubes.

The compromise value for  $R_f$  of 10 kohms that was finally arrived at keeps the current loss to a reasonable value (2.8 A) and allows a fall time of approximately 100 nsec from the 100 to 75% level.

With these values it was possible to obtain an RF output pulse with rise and fall times which are approximately the same (100 nsec maximum).

#### *Choice of switch tubes*

The choice of the switch tubes (Fig. 13-30) for the modulator was based upon a consideration of the following requirements:

1. A high-voltage rating compatible with the maximum beam voltage required for the klystron, with a reasonable safety margin.
2. A peak current capability, as determined by the maximum value of the current for the specified rise time and load.
3. A suitable plate resistance, which, of course, is related to the efficiency of the modulator and the anode dissipation of the tube. It is also a factor in determining the high-voltage power supply specifications.



4. Suitable drive characteristics, which are determined to a large extent by the input capacitance and the cutoff point of the tube as well as transconductance.
5. Flatness of the pulse obtainable. The characteristics of the tube play a major role at this point.
6. Freedom from arcing for extended periods of operation, taking into account that most vacuum tubes for pulse service suffer from this irregularity.
7. Minimal cost of replacement of a sizeable number of tubes on a year-round 24-hour basis. The economics play an important role when so many modulators are involved.

A tetrode was chosen in preference to a triode, because the grid drive power is considerably less for the tetrode—an important factor for fast rising pulses. Another reason for selecting the tetrode was because of the stringent pulse flatness requirement which could only be met by the tetrode tube type.

The tube decided upon was the 4PR1000A, which is an excellent tube when properly processed. The disadvantages in the choice of this particular tube are that three tubes have to be used in parallel to handle the current, and the high-voltage hold-off safety margin is on the low side. However, there are only a very limited number of tubes available in this high-voltage and current range.

Initially two 4PR1000A's were used in parallel. However, due to an unknown mechanism, possibly because of positive ion bombardment when the tubes are operated at or near the saturation knee of the  $e_p/i_p$  curve, the thoriated tungsten filaments are decarburized. This results in a steady decrease in peak current capability and at the same time in an increase in rise time of the beam voltage pulse and a shortened flat-top portion. A three-tube parallel arrangement alleviates this problem to some degree, because the load on each tube is decreased.

The main disadvantage of the third tube is the addition of its output capacitance to the stray capacitance of the circuit. There is also a small decrease in reliability of the equipment because of added complexity.

A developmental tube (Y448) with increased filament power and corresponding peak current output capability has been successfully tested and has shown satisfactory life expectancy under the present operating conditions. Two of these tubes are a satisfactory substitute for three 4PR1000H's.

It is clear that, at this time, no tube fully meets the SLAC requirements. Work aimed at improving performance and life expectancy is continuing.

#### *Driver circuit*

The driver circuit for the switch tubes is shown in Fig. 13-33. It consists of a delay line-controlled blocking oscillator  $V_1$  and a bootstrap amplifier  $V_2$ . Bias for both tubes is developed across a common cathode resistor and a

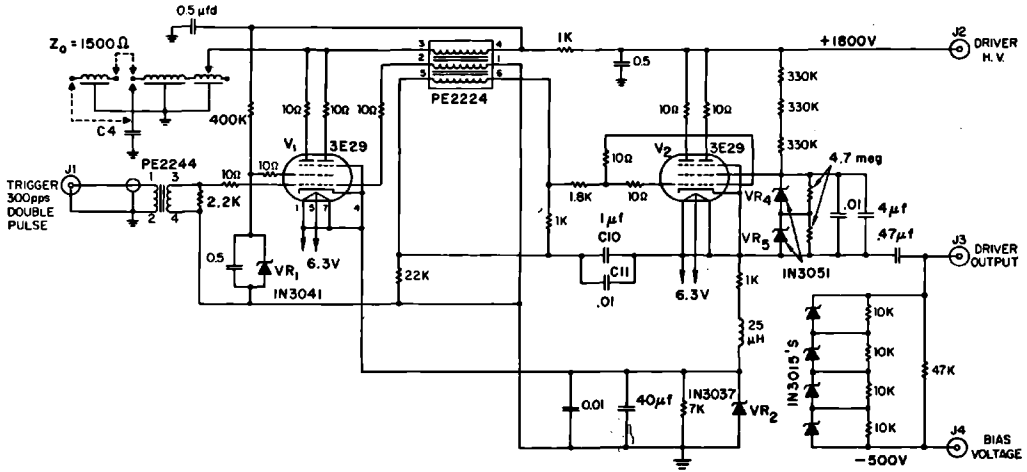


Figure 13-33 Sub-booster driver circuit.

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zener diode VR<sub>2</sub>. The screen voltage of V<sub>1</sub> is stabilized by VR<sub>1</sub>, and the bootstrap amplifier screen voltage is determined by the zener diodes, VR<sub>4</sub> and VR<sub>5</sub>.

Stabilization of these voltages is important in reducing the recovery time required by the blocking oscillator V<sub>1</sub>. A minimal recovery time is essential to meet the requirement for identical pulse shapes in pulse pairs at minimum separation (20 μsec).

The operation of the circuit is straightforward. A 50-V positive trigger at the first grid of V<sub>1</sub> results in an amplified negative pulse at the plate. This negative pulse, in turn, drives the control grid of the right-hand section more positive, through polarity reversal by the transformer. The anode begins to draw current through the pulse transformer which, in turn, drives the grid further positive, thus providing positive feedback. The right-hand section of V<sub>1</sub> is now fully turned on, and the negative pulse at the plates progresses down the delay line, is reflected by C<sub>4</sub>, and travels back with opposite polarity through the transformers turning the tube off via its grid and returning it to a stable condition.

The two-way travel time along the delay line determines the width of the pulse. A fine adjustment for the delay is provided, and long-term stability is obtained by the excellent temperature characteristics of the line.

The tertiary winding on the blocking oscillator transformer is connected to the grids of the bootstrap amplifier, V<sub>2</sub>. The output of the blocking oscillator is effectively applied between the cathode and grids of V<sub>2</sub> through the capacitors C<sub>10</sub> and C<sub>11</sub>.

The bootstrap cathode follower V<sub>2</sub> provides a positive output pulse for a positive input. Stabilization of the screen voltage reduces pulse droop and makes it feasible to obtain two very nearly identical pulses in a pair.

The output pulse is capacitively coupled to the grids of the switch tubes and is superimposed on their cutoff bias voltage. Bias voltage is provided by a highly regulated power supply and applied to the grids through a series resistor.

The amplitude of the drive pulse can be clipped to approximately 800 V by a zener diode arrangement to limit overshoot, ripple, and droop to a very low level. The switch tubes also help to clip the pulse when their grids are driven sufficiently positive.

The plate voltage for the driver unit is supplied from a highly regulated power supply.

### *Power supplies*

The power supplies used in the sub-booster modulator are divided into two groups: (1) Main high-voltage power supply with a separate high-voltage regulator and (2) three separate high-voltage supplies, in one package, but with individual controls and meters.

The various outputs are

Bias: 0 to  $-800$  V, 0–3 mA  
 Driver: 0 to  $+2100$  V, 0–27.5 mA  
 Screen: 0 to  $+2100$  V, 0–47.5 mA

These supplies are very well-regulated to obtain the required stability of the RF output pulse under varying ac line conditions. Temperature compensation in the regulating circuits of these supplies minimizes the instability caused by the widely varying temperatures in the gallery where this equipment is located.

For increased reliability, silicon solid-state devices are used in these power supplies, with the exception of the series-regulating tubes.

The power supplies are protected from overload conditions, such as shorts in a damaged switch tube, by a current-limiting circuit.

### *Main high-voltage power supply*

The main high-voltage power supply consists of a single phase, full wave bridge rectifier with a series regulator. Its output dc level is regulator-controlled in the voltage range from 24 to 29 kV. Below 24 kV the output is controlled by varying the rectifier ac input by a motor-driver variable transformer.

The nominal output of the unregulated section is 32 kV at 40 mA and the maximum output after the regulator is 29 kV at the same current rating. Overcurrent and overvoltage protection is provided for the power supply and its associated pulser circuit, complete with automatic recycling. This enables the modulator to recycle after a momentary overcurrent condition, i.e., arcing in a switch tube. If more than three faults occur in a 5-min period, the modulator

will be turned off, in which case it must be reset manually. The motor-driven variable transformer is interlocked to prevent turn-on unless it is set for minimum output.

#### *High-voltage regulator circuit*

The high-voltage regulator circuit is of the conventional series type, with one special feature. All amplifier and low-voltage power supply circuits are near ground potential, which makes servicing and trouble shooting not quite as dangerous as in circuits floating at the 30-kV level. This is made possible by the application of a 6BK4A shunt voltage regulator tube between the last amplifier stage and the grid of the 4PR400A series regulator.

The 4PR400A tube and its screen supply are the only components mounted on a floating chassis. This regulator will only function in a limited range, 24–29 kV, thus eliminating the need for a larger tube with a considerably greater anode dissipation rating to accommodate a larger voltage range. The 24–29-kV range is ample for this application.

#### **References**

- 1 G. N. Glasoe and J. V. Lebacqz, eds., *Pulse Generators, Mass. Inst. Technol. Radiation Lab. Series*, Vol. 5, McGraw-Hill, New York, 1948.
- 2 R. W. Bradford, "Hydrogen Thyatron Performance in the SLAC Two-Mile Accelerator," Rept. No. SLAC-PUB-192, Stanford Linear Accelerator Center, Stanford University, Stanford, California (May 1966).
- 3 T. F. Turner, "An Improved Pulse Transformer for High-Voltage Applications," Rept. No. ML609, Microwave Laboratory, Stanford University, Stanford, California (May 1959).
- 4 P. R. Gillette, K. W. Henderson, K. Oshima, and R. M. Rowe, "Pulse Transformer Design and Test Methods," Final Report, Part I (AD 79 221), Part II (AD 79 222), Part III (AD 79 223), Project No. 782, Stanford Research Institute, Menlo Park, California (May 1959).
- 5 K. Dedrick, "Measurement of High Voltage Pulses with Co-axial Voltage Divider," Rept. No. ML-556, Microwave Laboratory, Stanford University, Stanford, California (1958).
- 6 W. R. Fowkes and R. M. Rowe, *IEEE Trans. Instrumentation and Measurements* IM-15, p. 284 (December 1966).